Compal Confidential

EFL50/ EFT51 Schematics Document

Intel Dothan/ Celeron M/ Alviso GM(PM) / DDR-2 / ICH6-M

(Daughter Card: ATi M24P/ M26P)

2005 / 03 / 08 (DVT)

Rev:0.2

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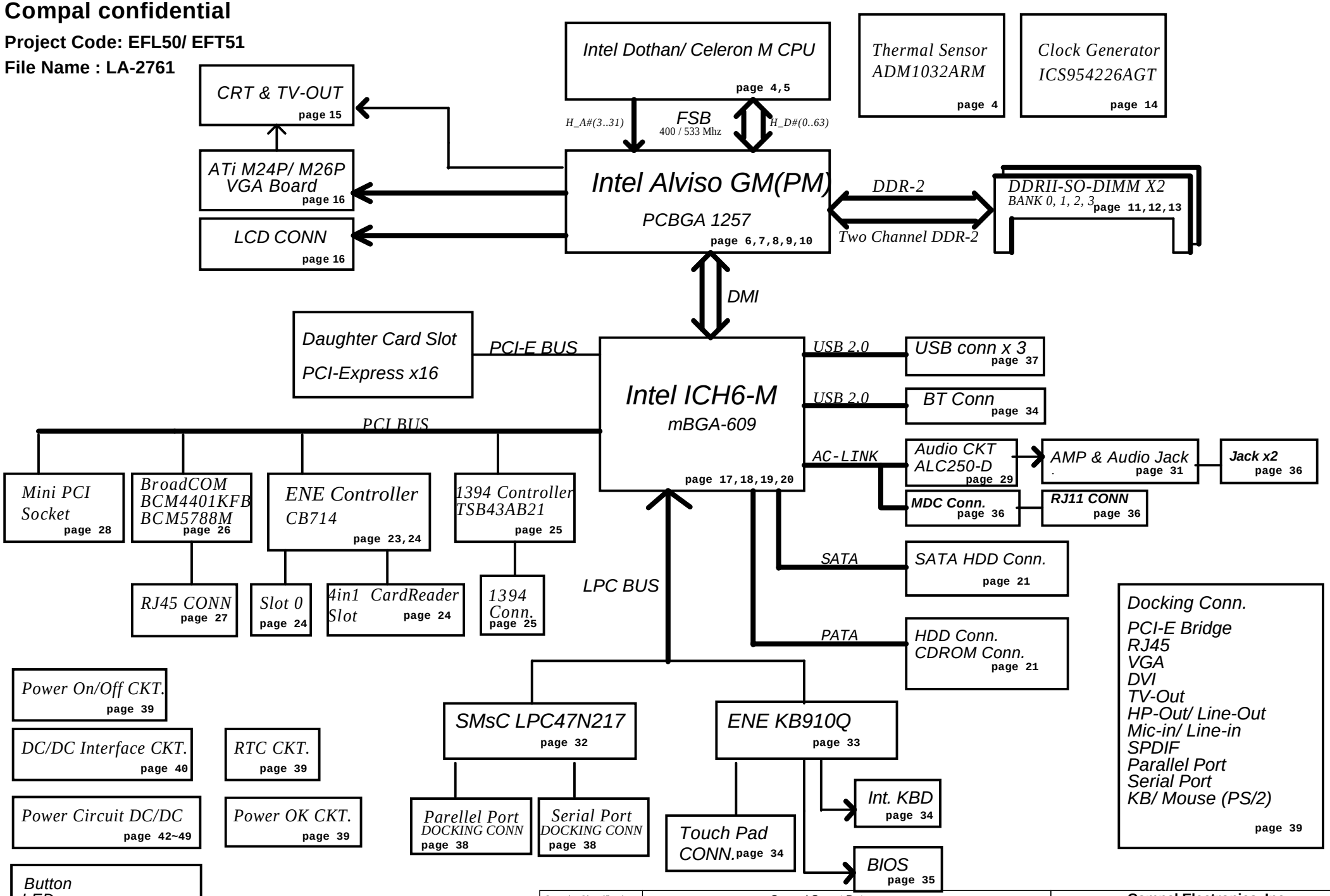
Project Code: EFL50/ EFT51

File Name : LA-2761



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Voltage Rails

Power Plane	Description	S1	S3	S4/ S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+DDRVTT	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON*
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+DDRVCC	1.8V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+5VMOD	5V switched power rail for Module Bay	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA/PIRQB
1394	AD16	0	PIRQE
SD	AD20	2	PIRQA/PIRQB
Mini-PCI	AD18	1	PIRQG/PIRQH
LAN	AD17	3	PIRQF

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
(24C04)	1011 000Xb

EC SM Bus2 address

Device	Address
ADM1032	1001 110X b

ICH6M SM Bus address

Device	Address
Clock Generator (ICS 954226AGT)	1101 001Xb
DDRII DIMM0	1001 000Xb
DDRII DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra / Rc	100K +/- 5%

Board ID	Rb / Rd	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

SKU ID Table

SKU ID	SKU
0	
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA	GM@
Discrete	PM@
LAN 10/100	4401@
LAN GIGA	5788@
1 Spindle	1S@
2 Spindle	2S@
2 Spindle with SATA	2SS@
2 Spindle with PATA	2SP@
1 Spindle with SATA	1SS@
1 Spindle with PATA	1SP@
With Docking	WD@
Without Docking	ND@
With 1394	1394@
With 1394 4pin	1394<4>@
With 1394 6pin	1394<6>@

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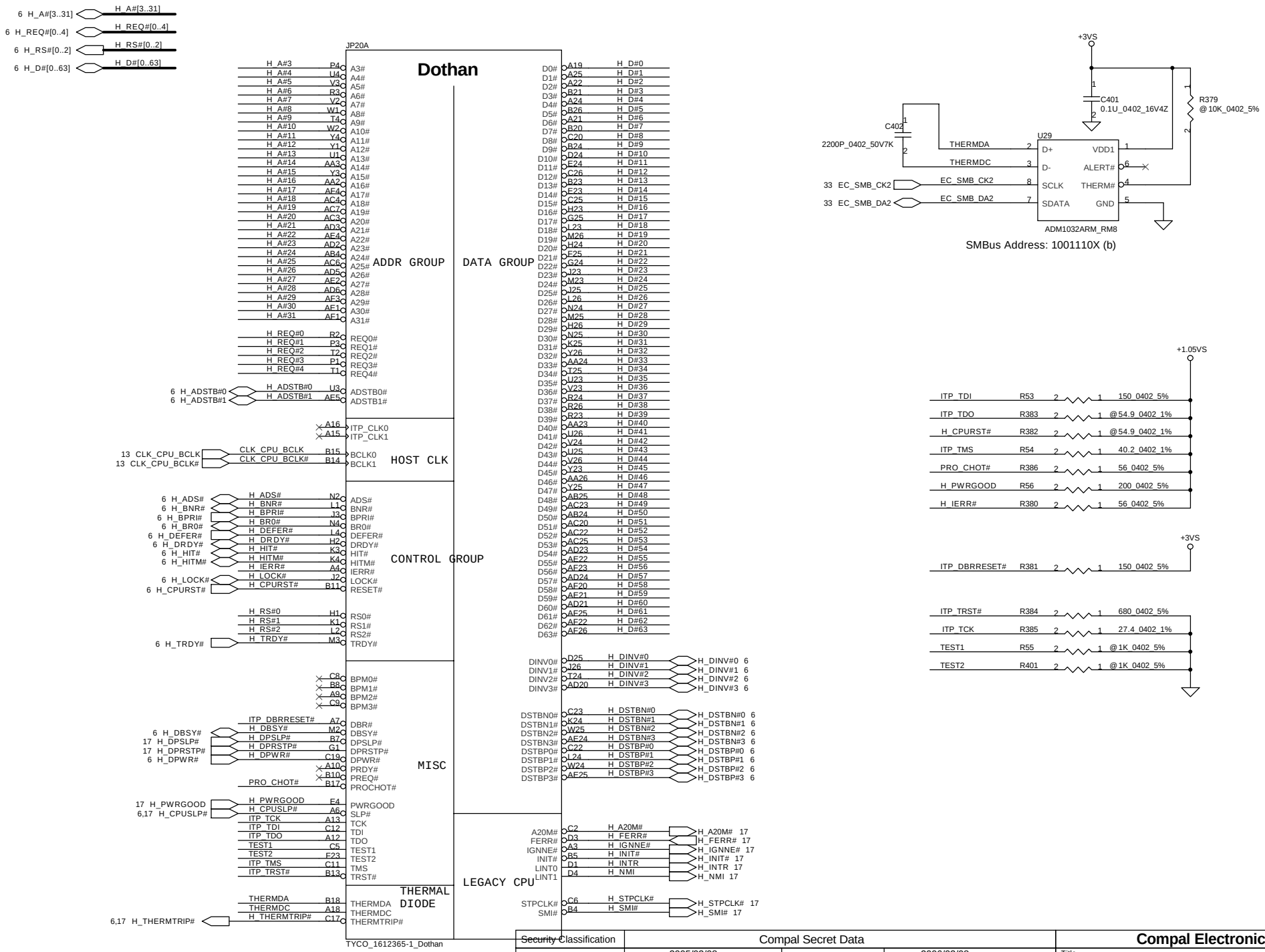

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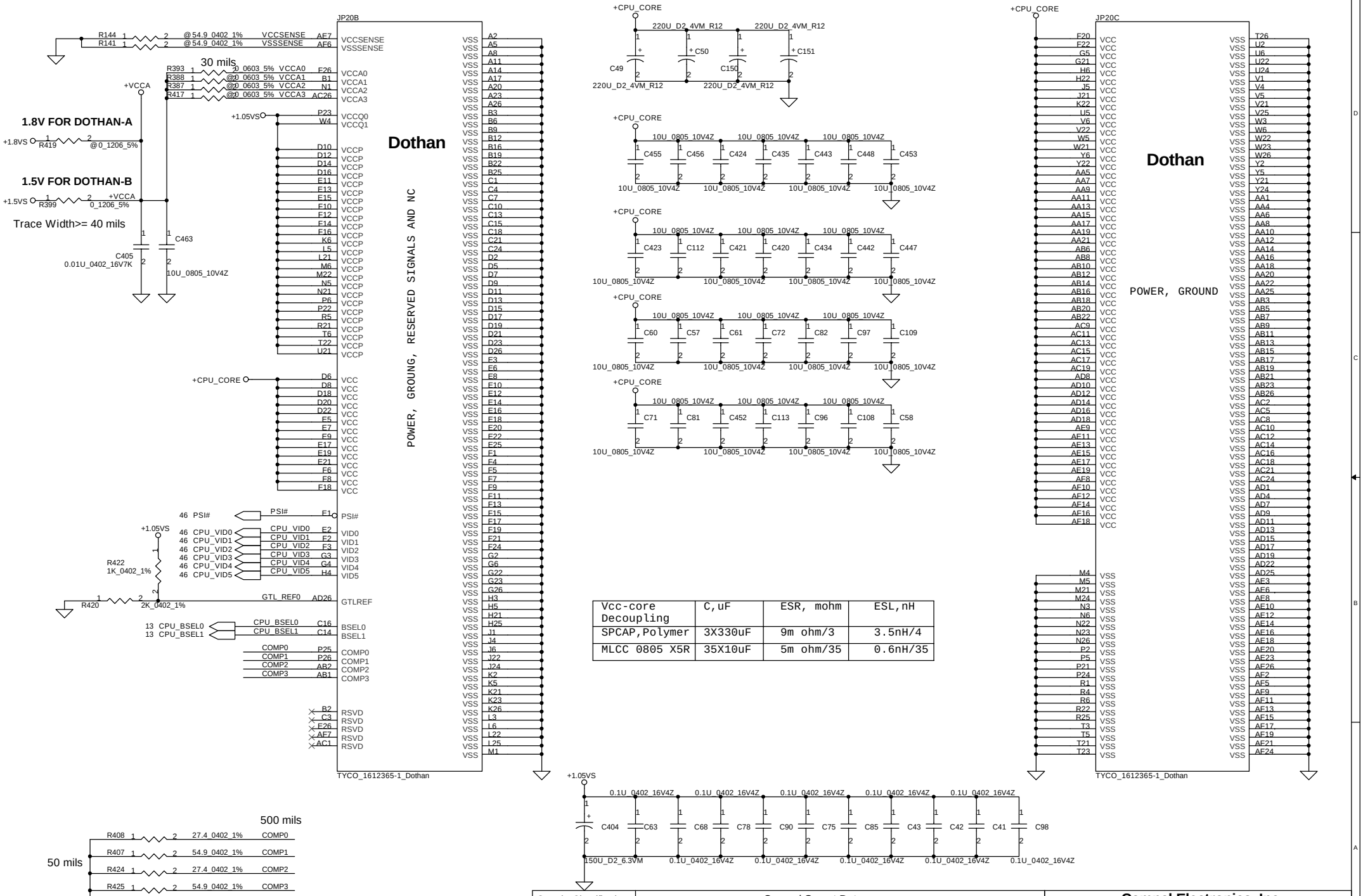

Vcc-core Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	3X330uF	9m ohm/3	3.5nH/4
MLCC 0805 X5R	35X10uF	5m ohm/35	0.6nH/35

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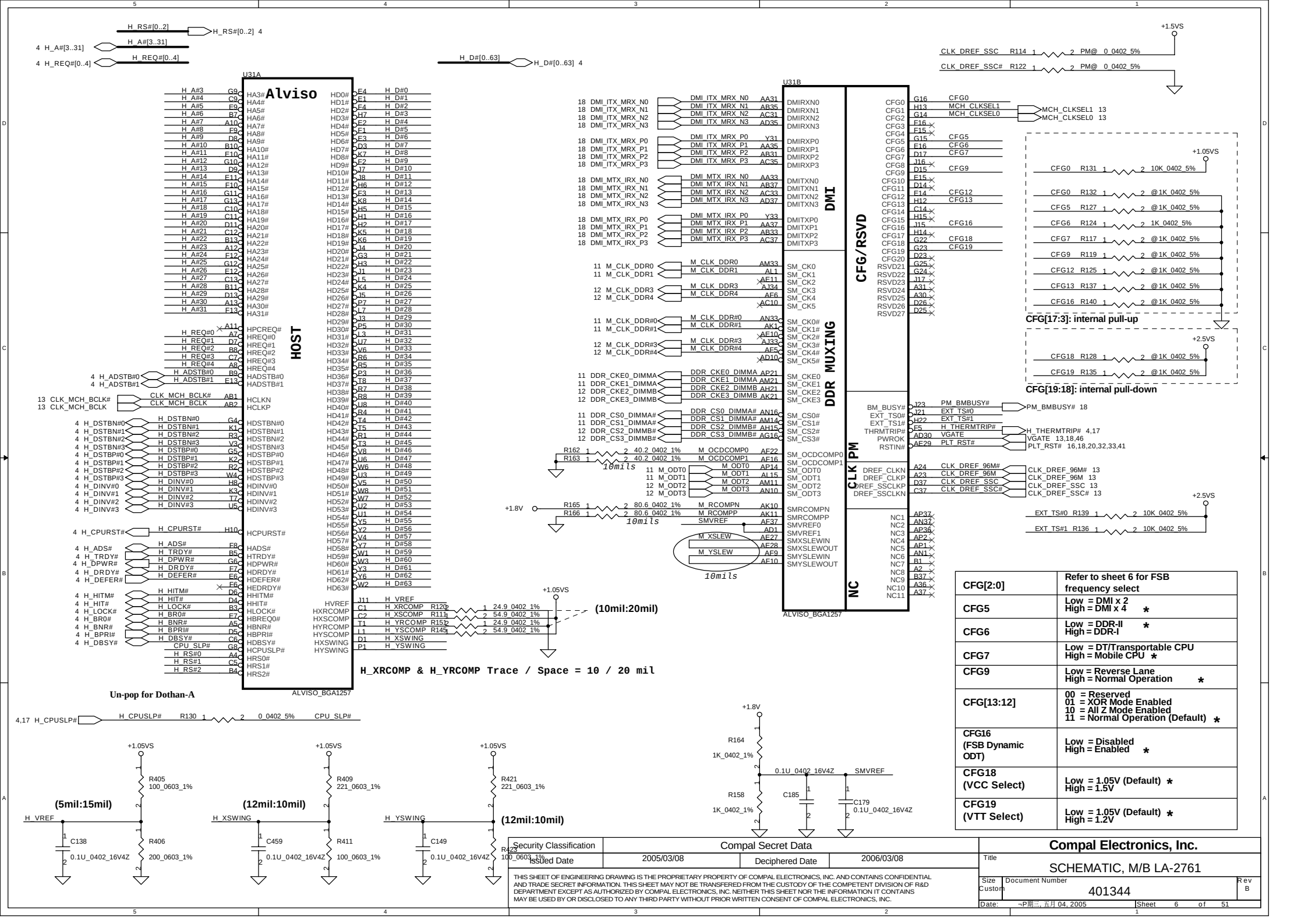

CFG[2:0]	Refer to sheet 6 for FSB frequency select
CFG5	Low = DMI x 2 High = DMI x 4 *
CFG6	Low = DDR-II * High = DDR-I
CFG7	Low = DT/Transportable CPU High = Mobile CPU *
CFG9	Low = Reverse Lane High = Normal Operation *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *
CFG18 (VCC Select)	Low = 1.05V (Default) * High = 1.5V
CFG19 (VTT Select)	Low = 1.05V (Default) * High = 1.2V

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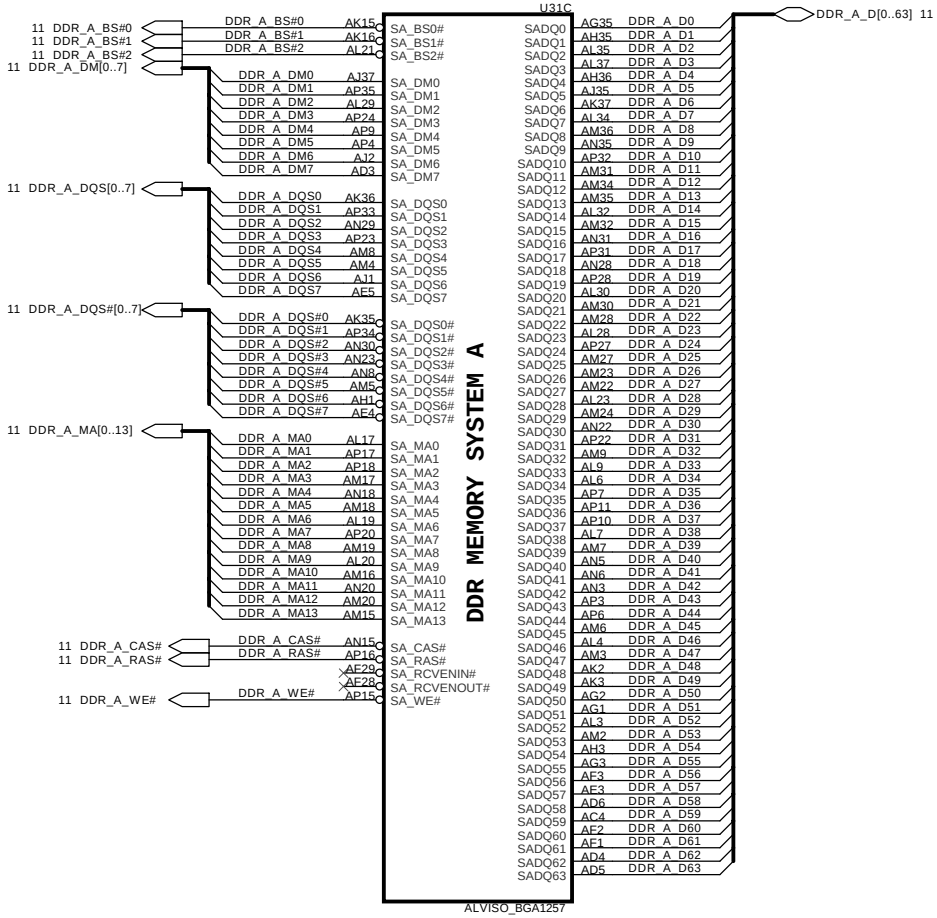

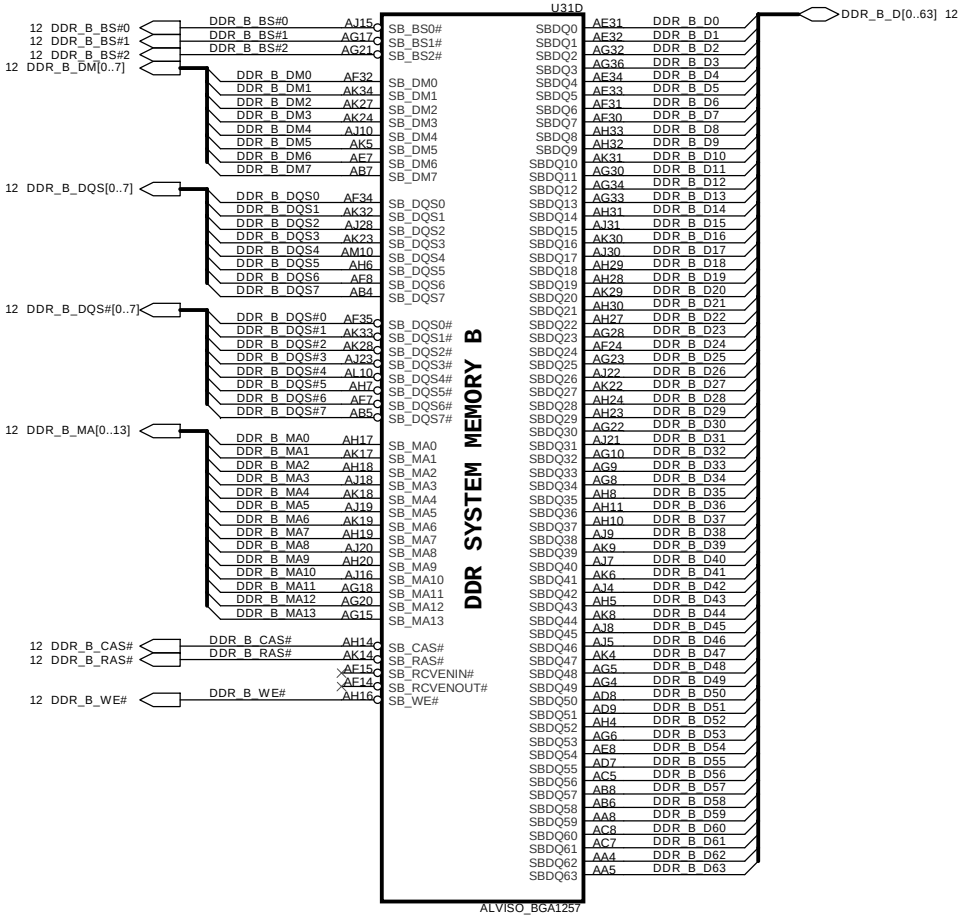

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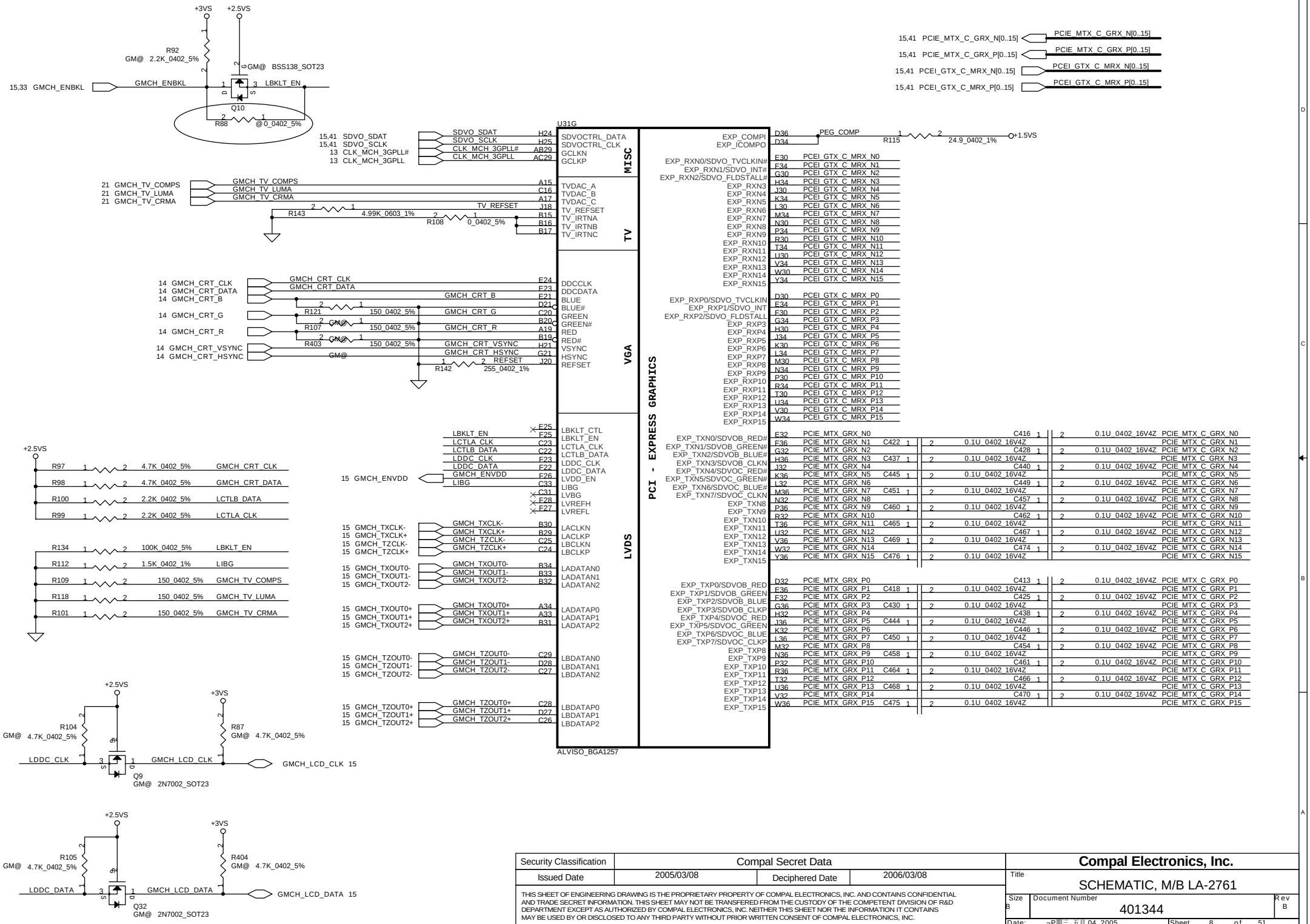

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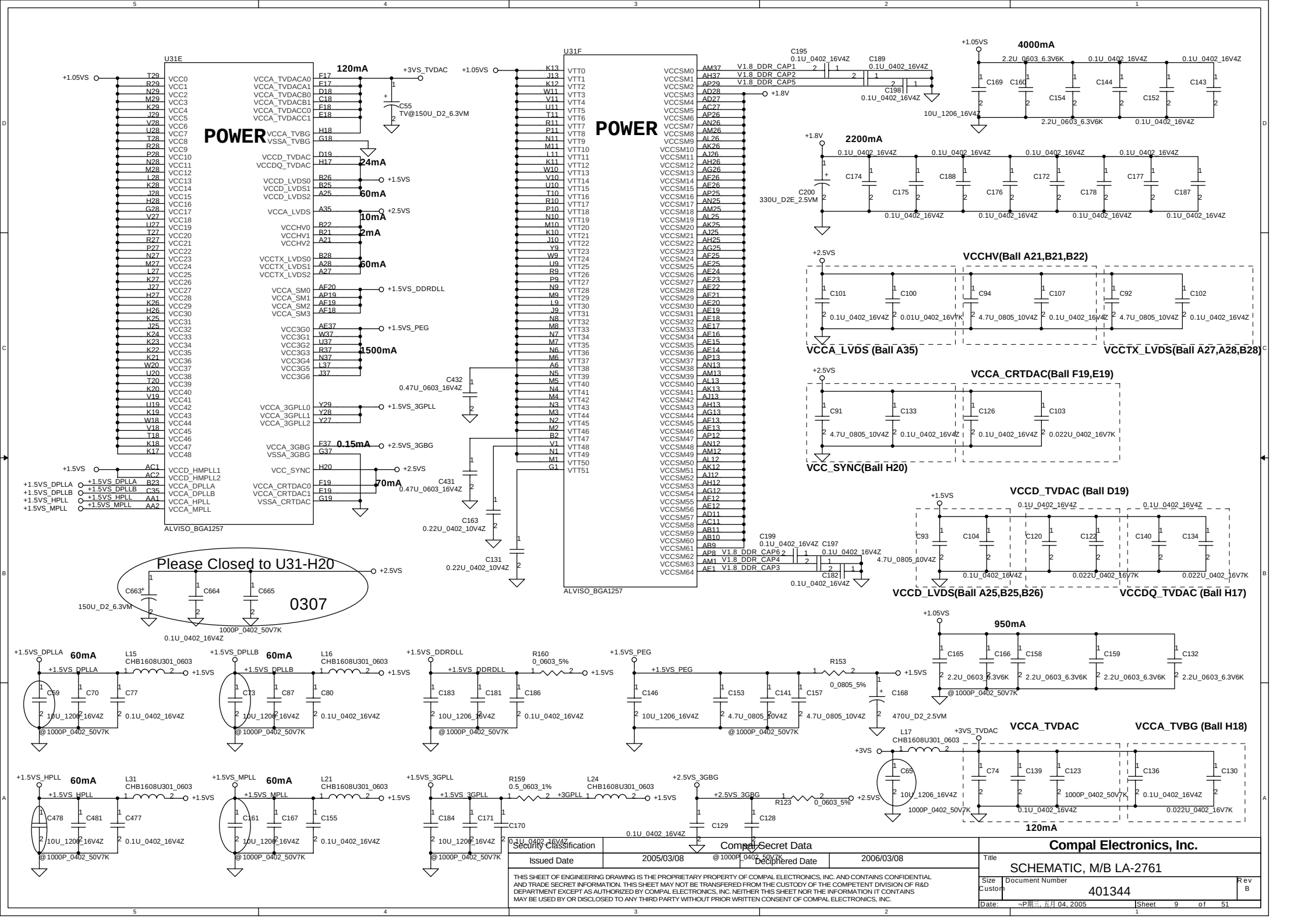

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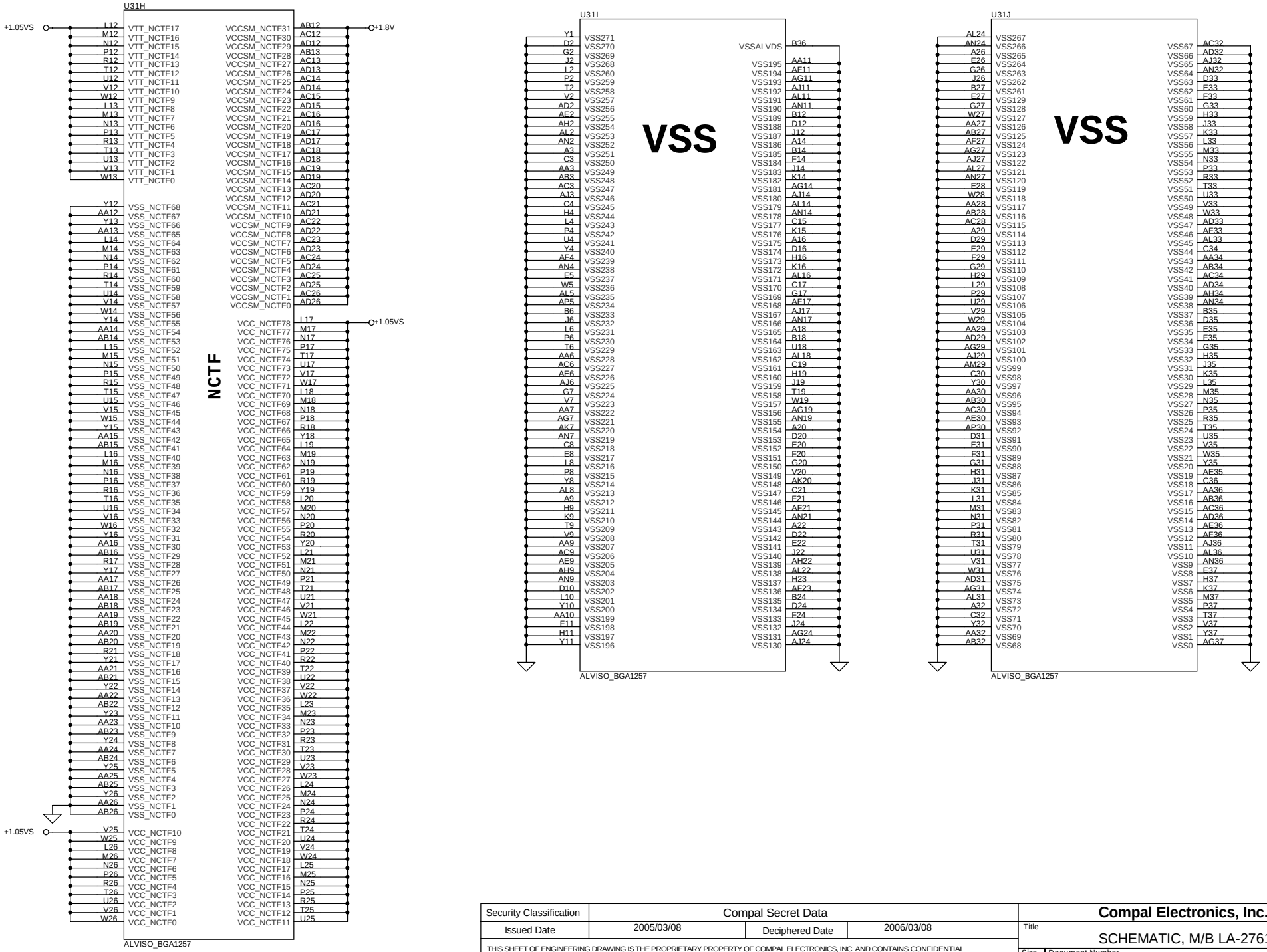

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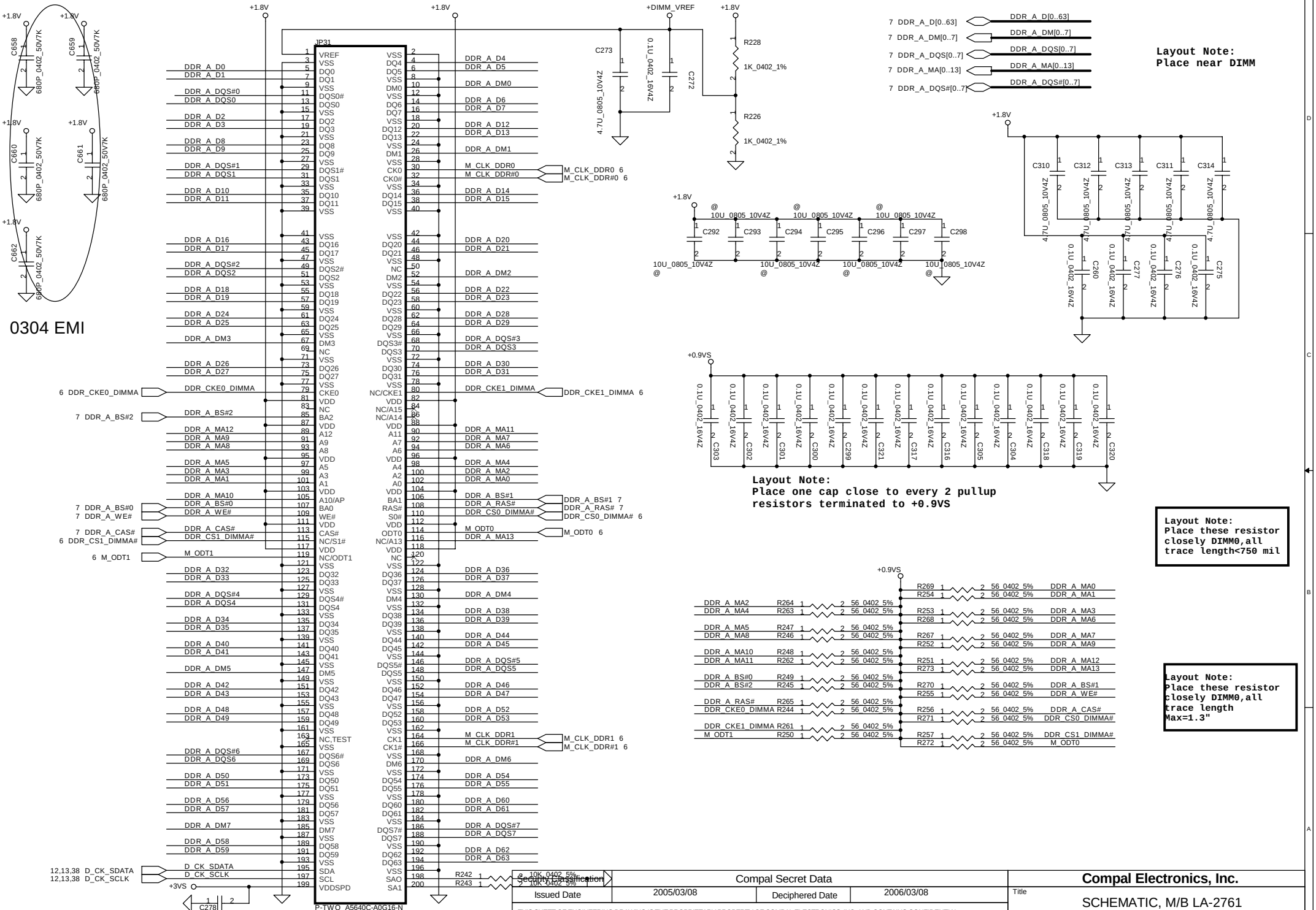
0304 EMI
JP31
P-TWO_A5640C-A0G16-N
Address: 1001 000X b
Layout Note:
Place near DIMM
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS
Layout Note:
Place these resistor closely DIMM0,all trace length<750 mil
Layout Note:
Place these resistor closely DIMM0,all trace length Max=1.3"
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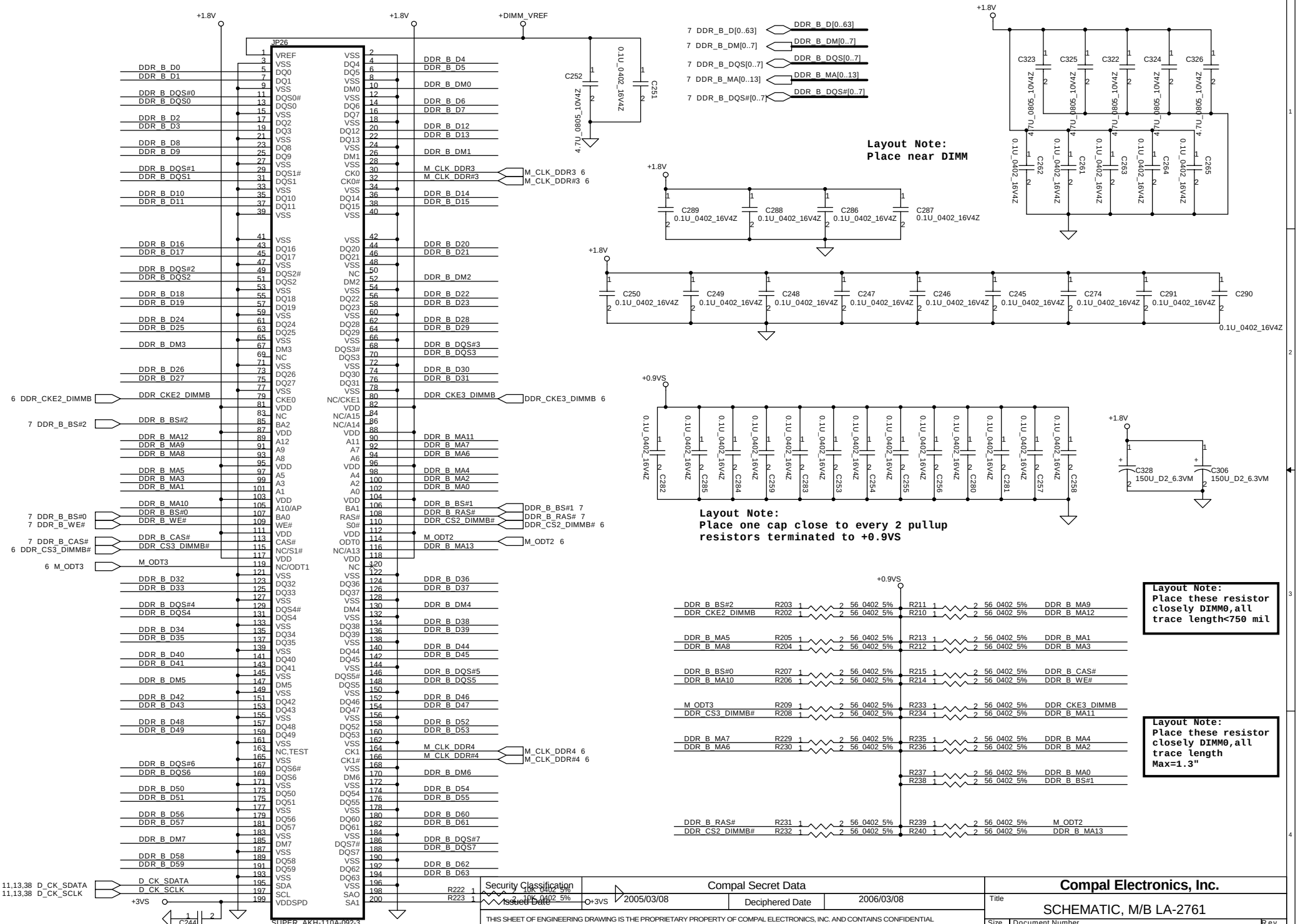

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Clock Generator

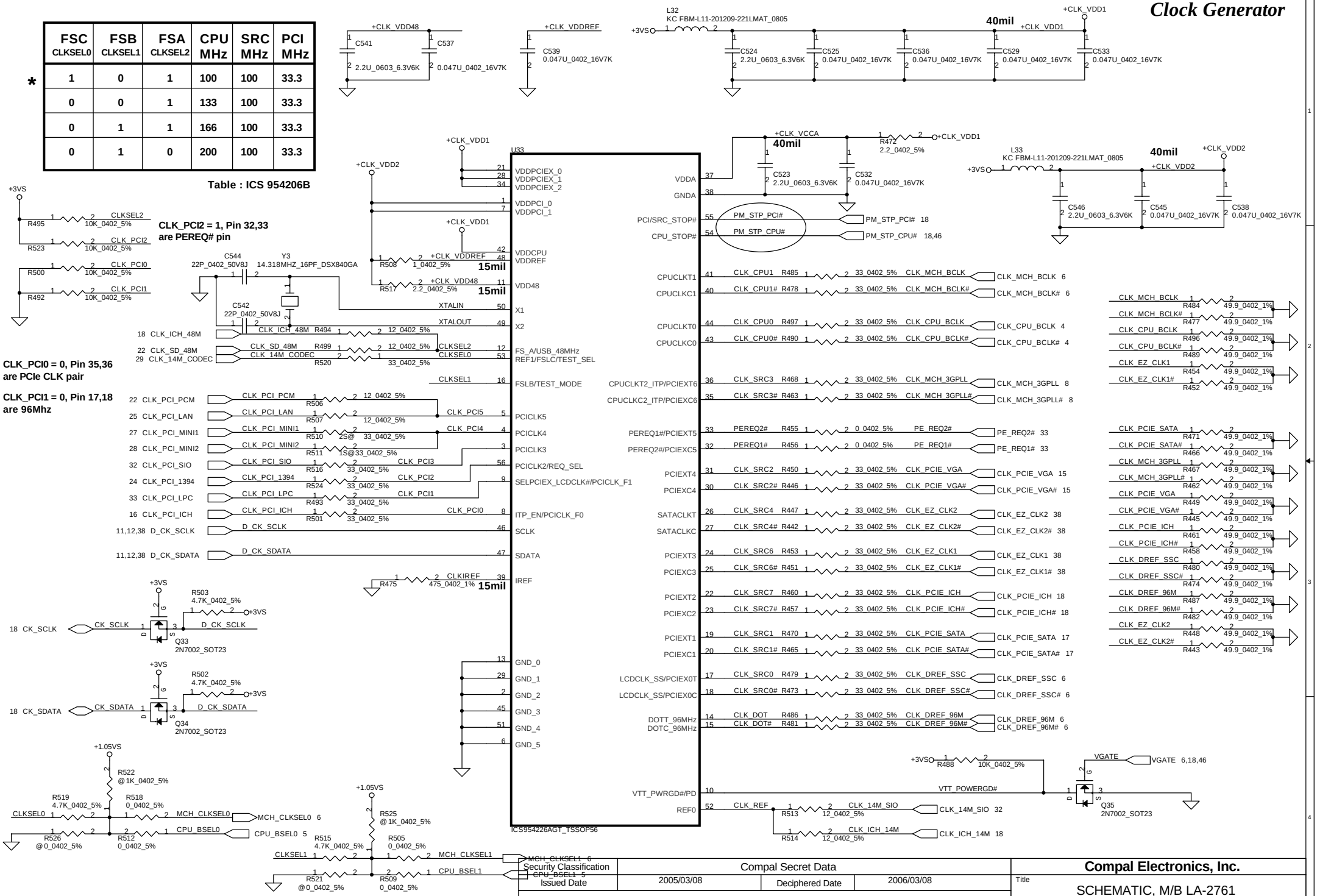
	FSC CLKSEL0	FSB CLKSEL1	FSA CLKSEL2	CPU MHz	SRC MHz	PCI MHz
*	1	0	1	100	100	33.3
	0	0	1	133	100	33.3
	0	1	1	166	100	33.3
	0	1	0	200	100	33.3

Table : ICS 954206B

CLK_PCI2 = 1, Pin 32,33 are PEREQ# pin

CLK_PCI0 = 0, Pin 35,36 are PCIe CLK pair

CLK_PCI1 = 0, Pin 17,18 are 96Mhz



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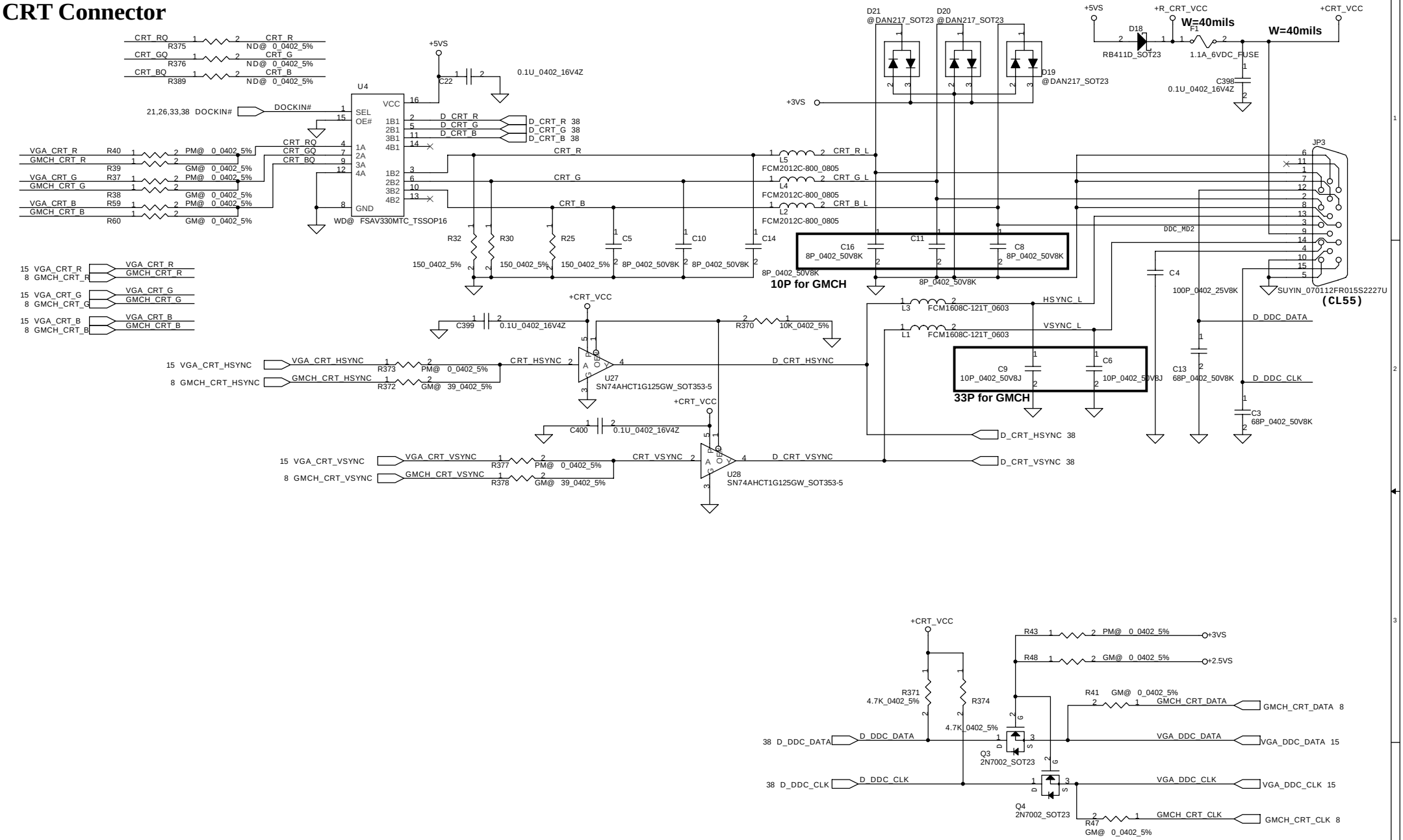
CRT Connector



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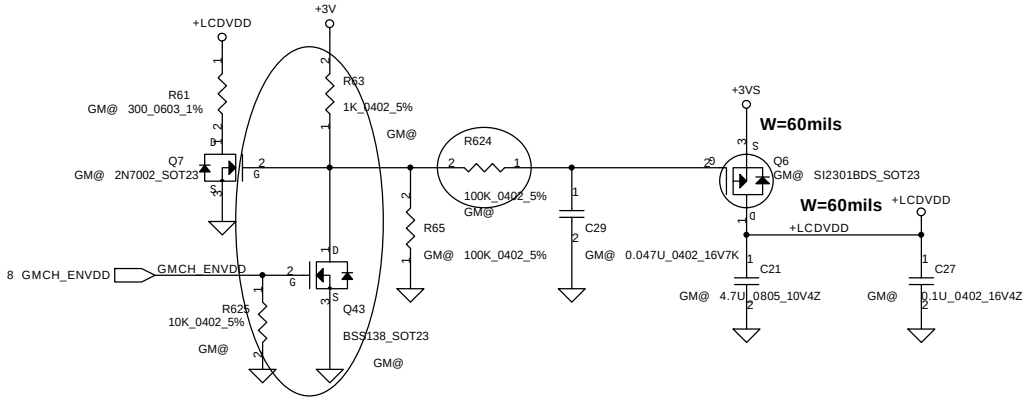
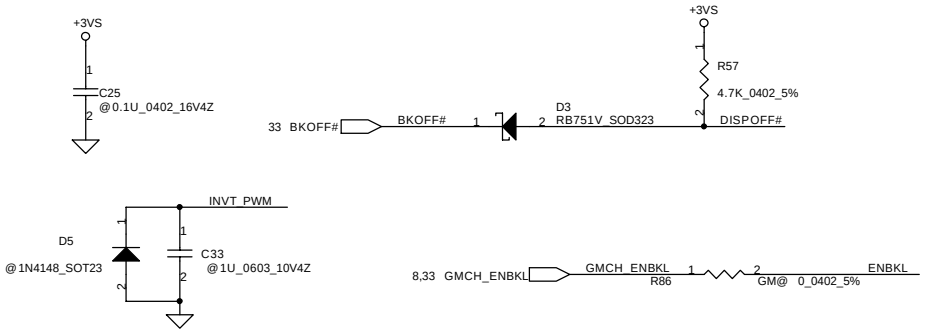
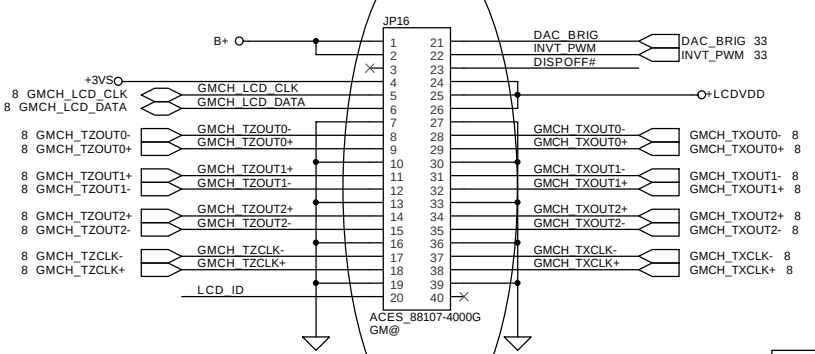
LCD POWER CIRCUIT

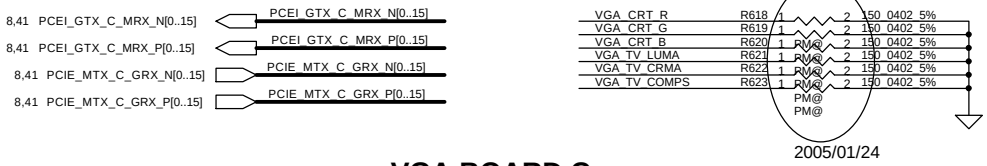




LCD/PANEL BD. Conn.

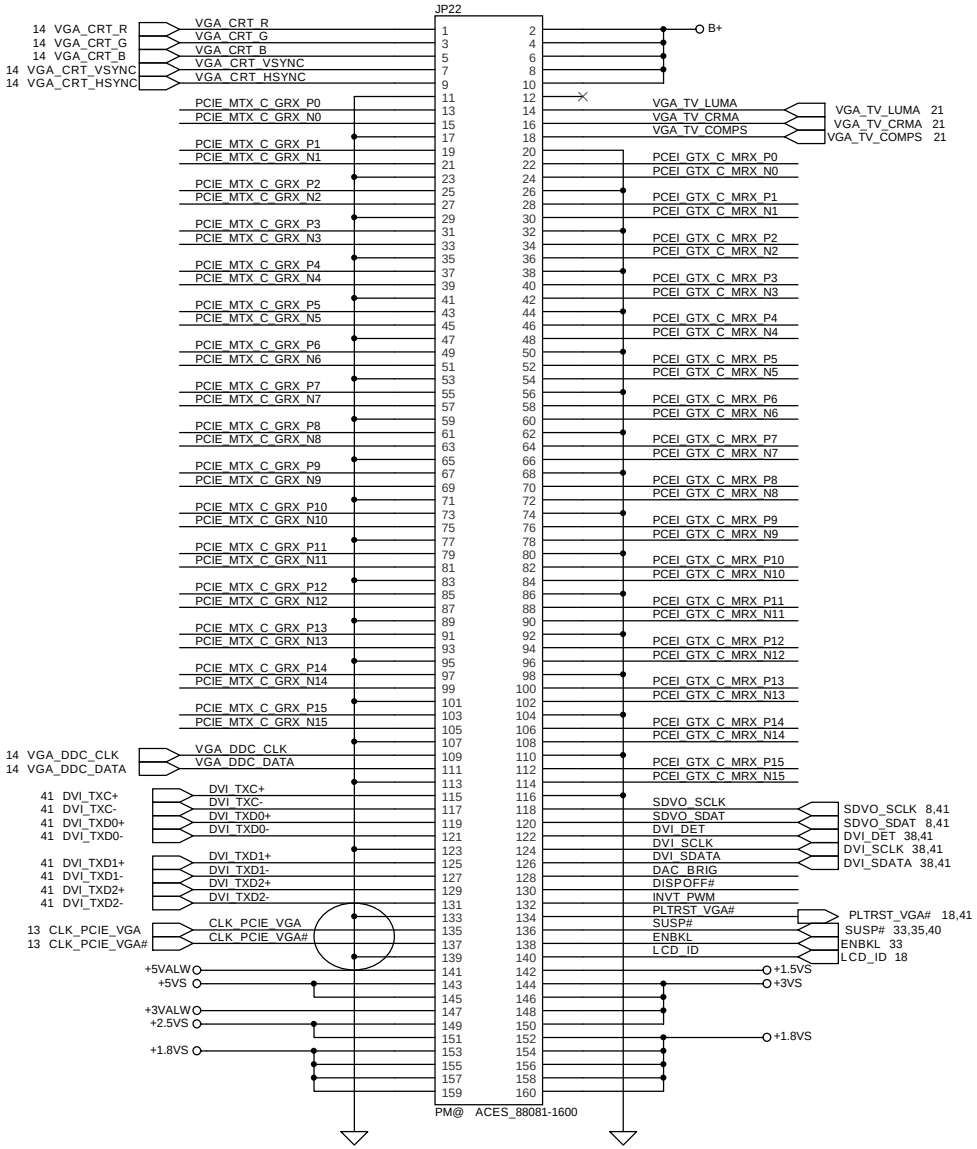


Reverse for Layout



2005/01/24

VGA BOARD Conn.



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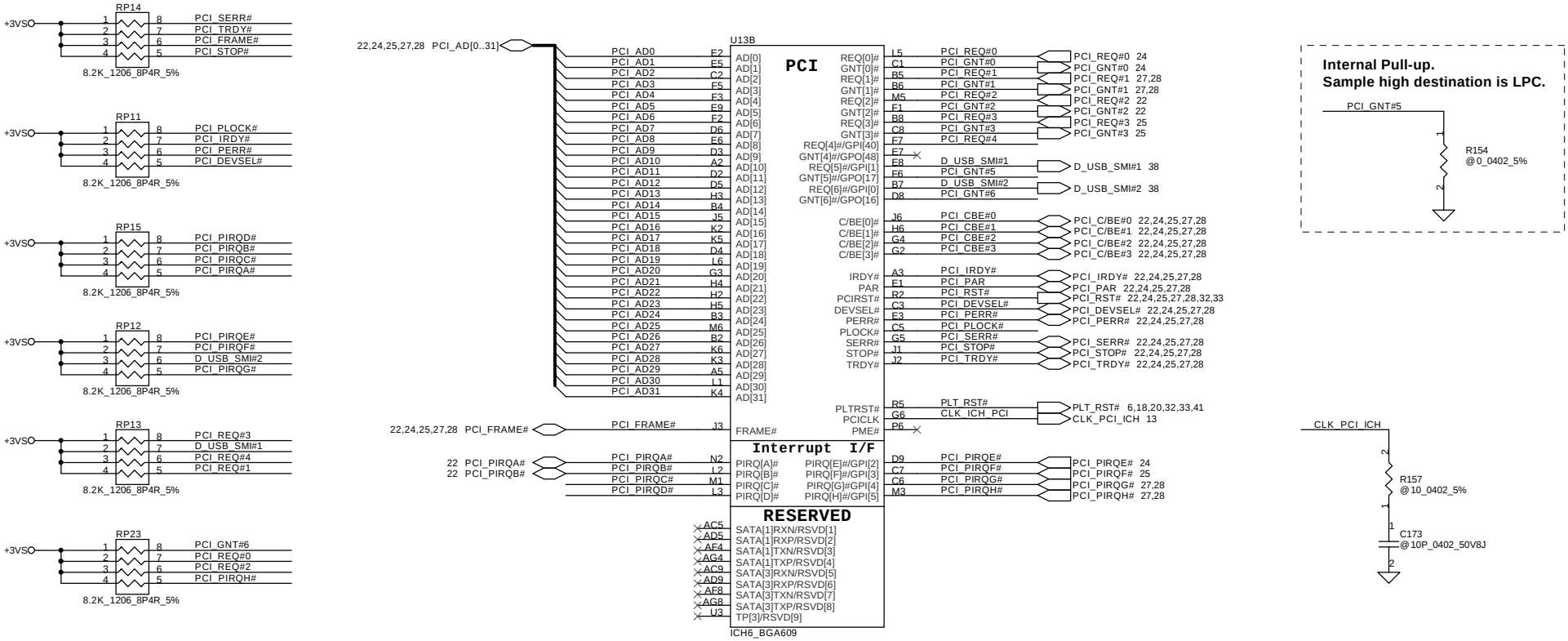

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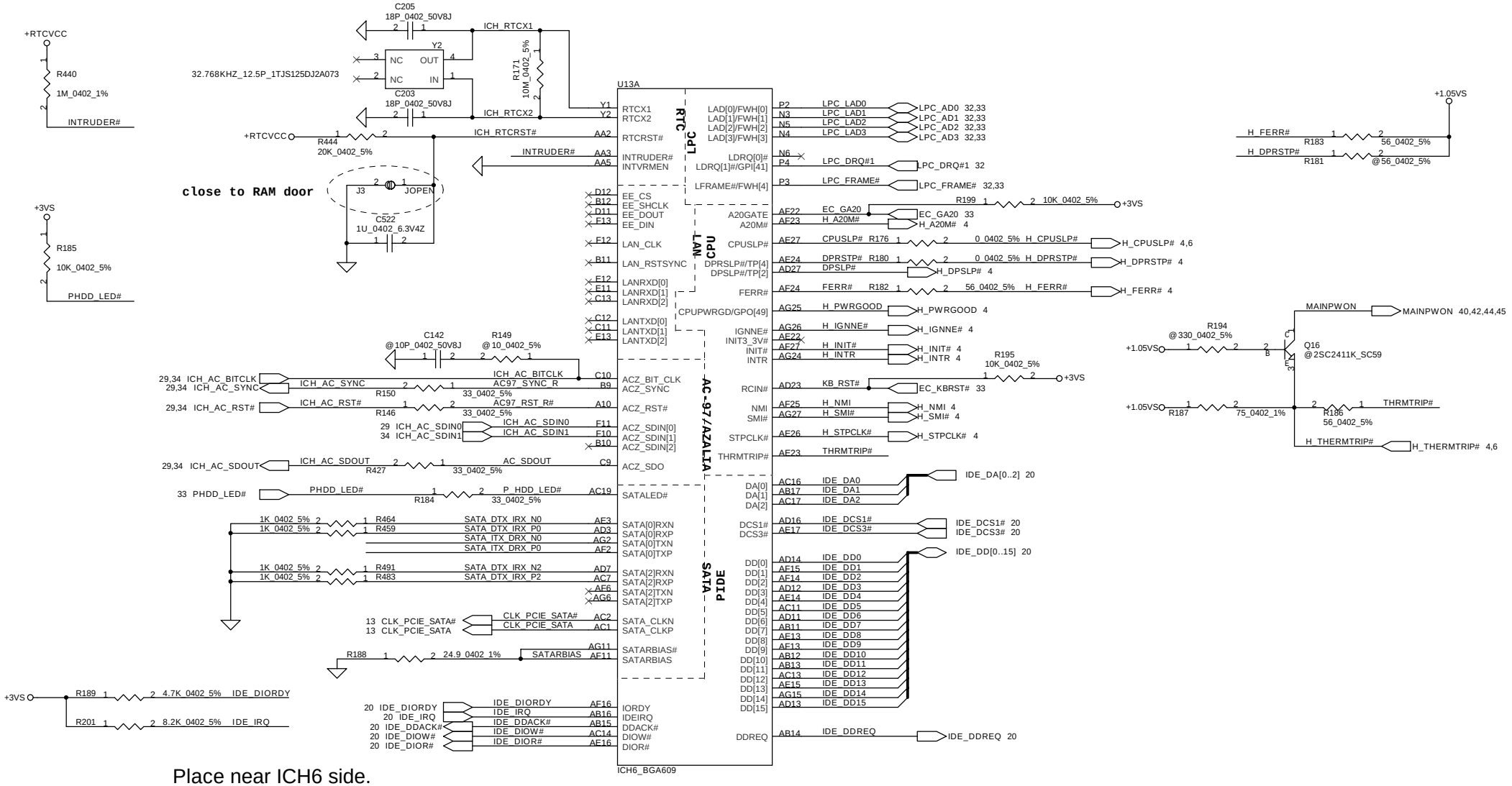

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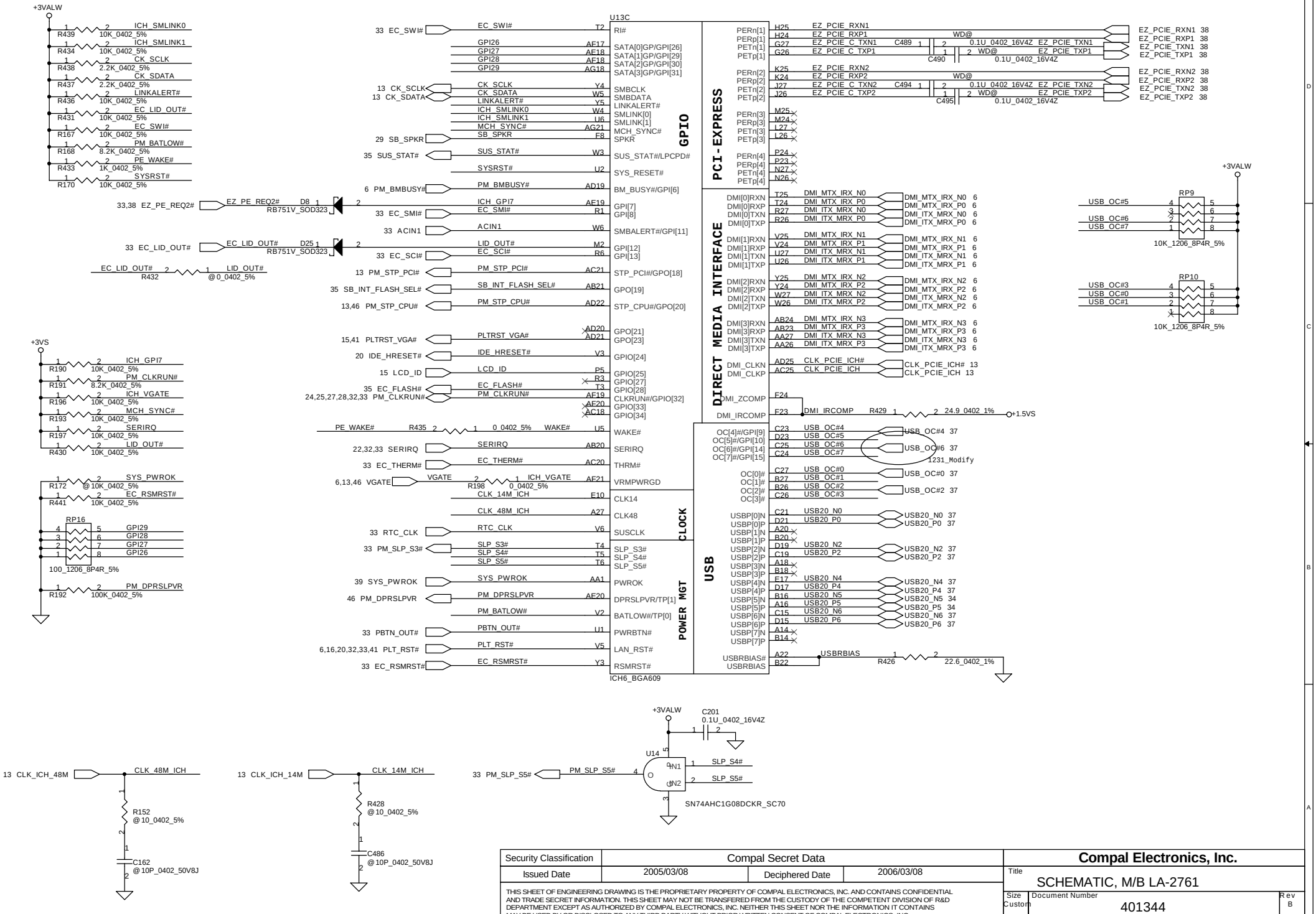

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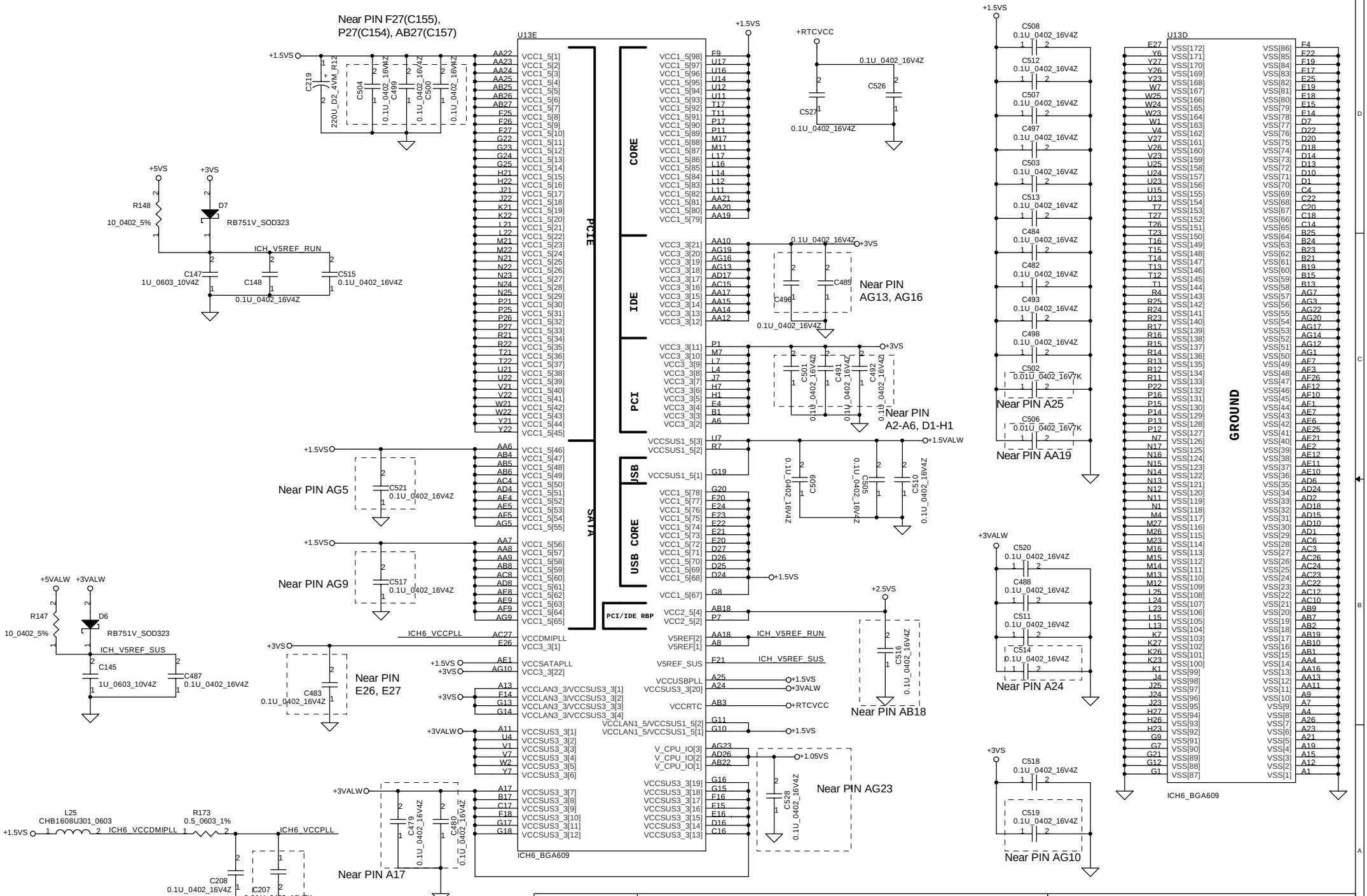

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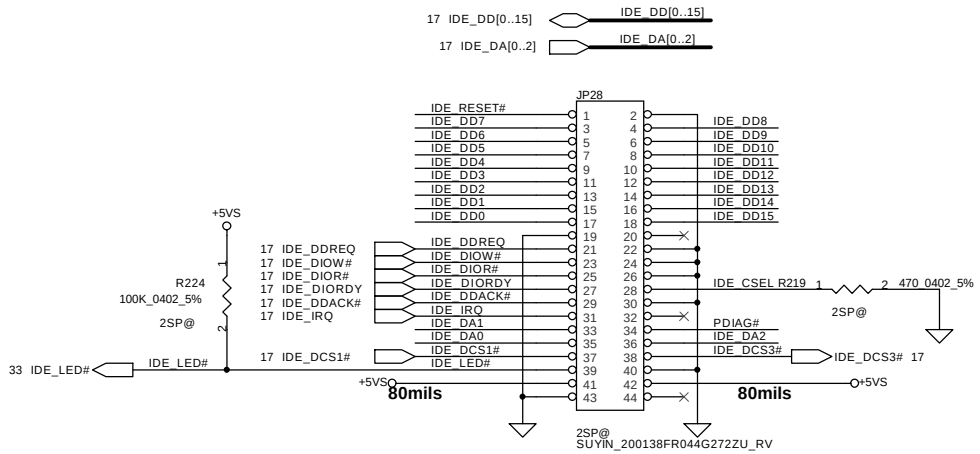
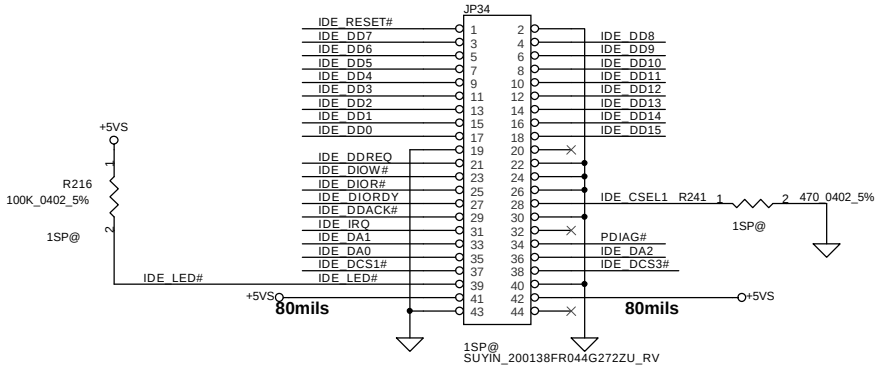
HDD CONN

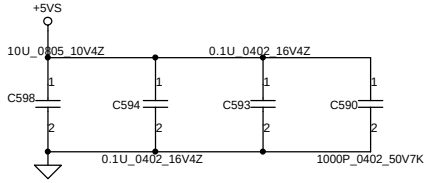


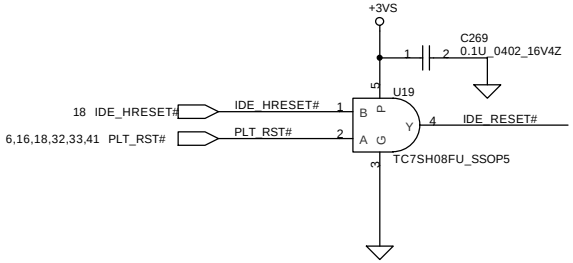
For 2 Spindle

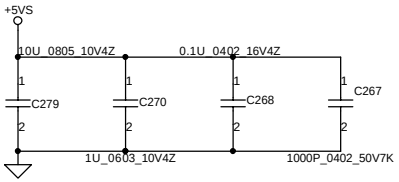
HDD CONN



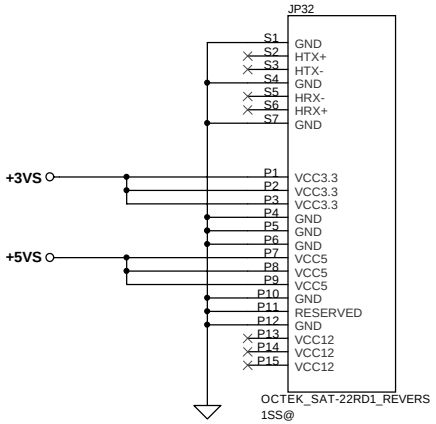
For 1 Spindle







SATA HDD CONN



For 1 Spindle

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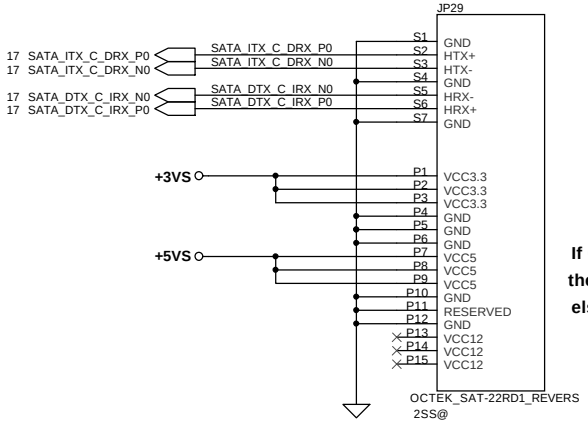
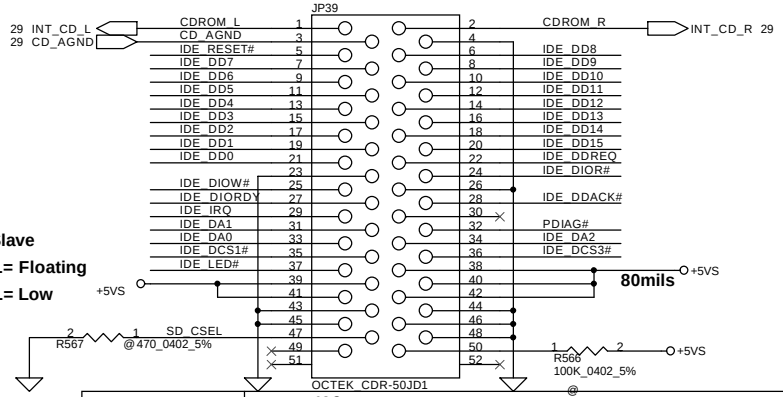


For 2 Spindle

CDROM CONN



If CDROM is Slave
then SD_CSEL= Floating
else SD_CSEL= Low

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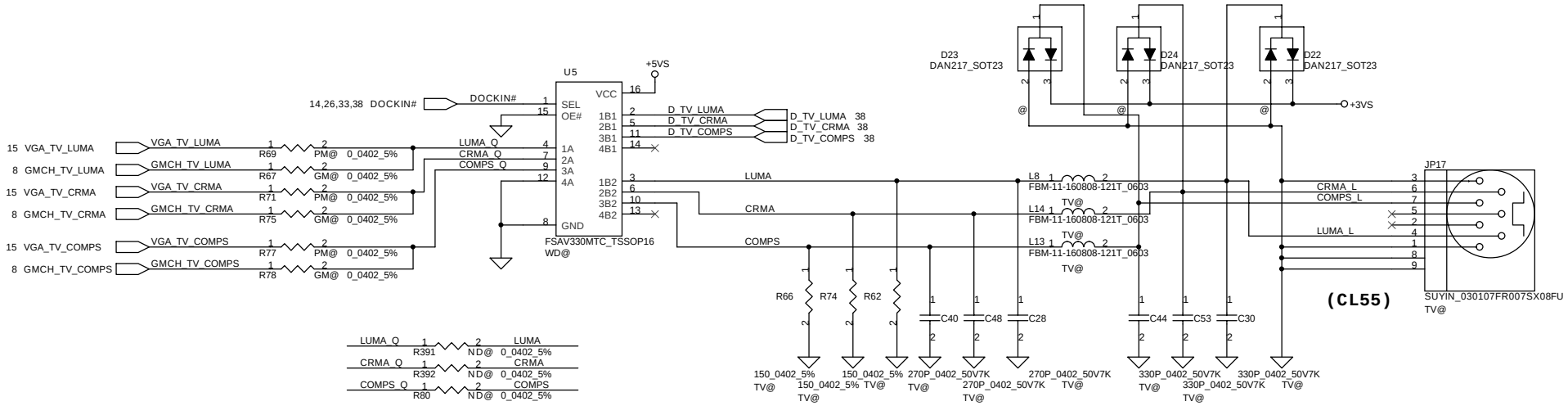

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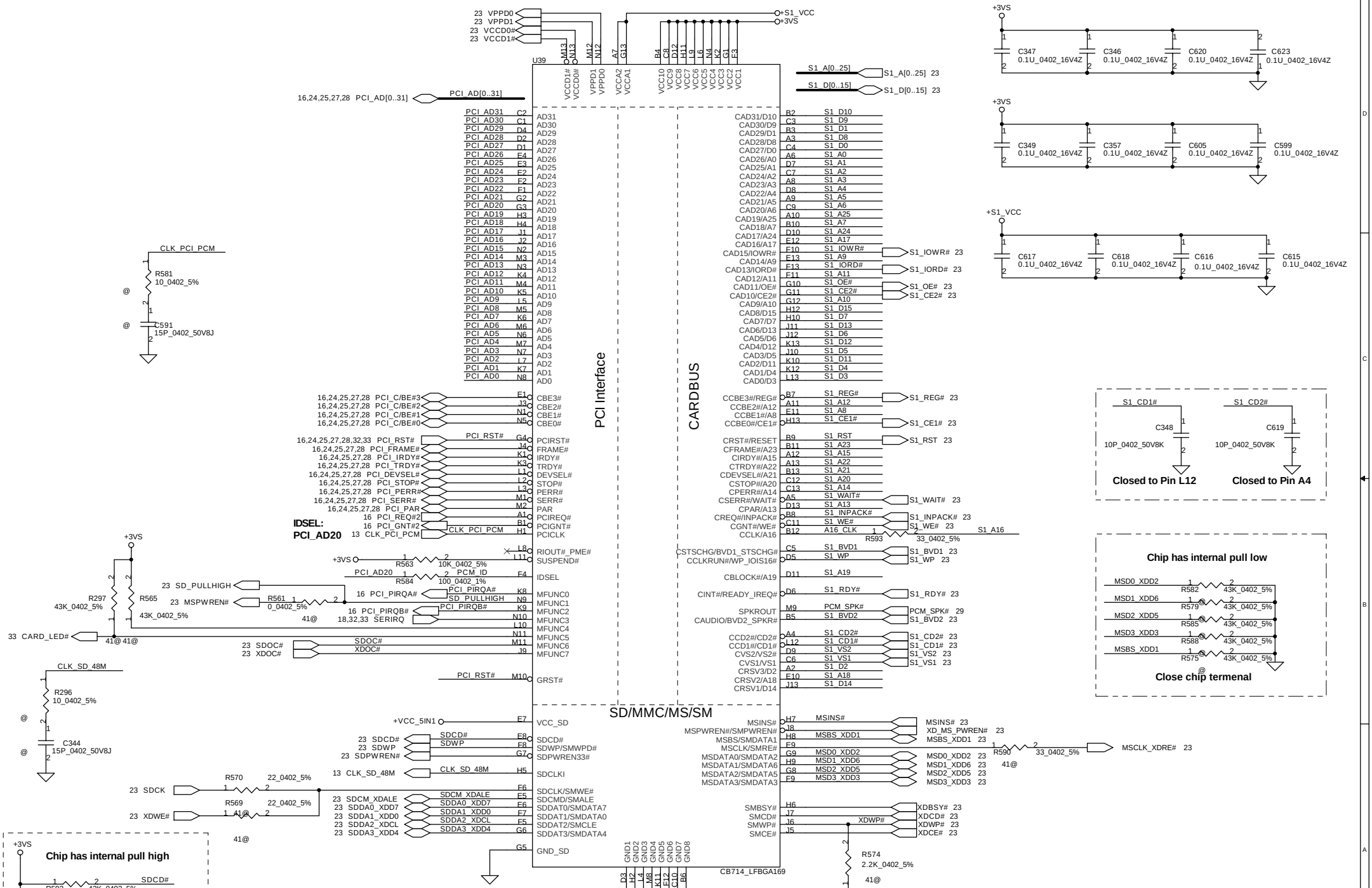

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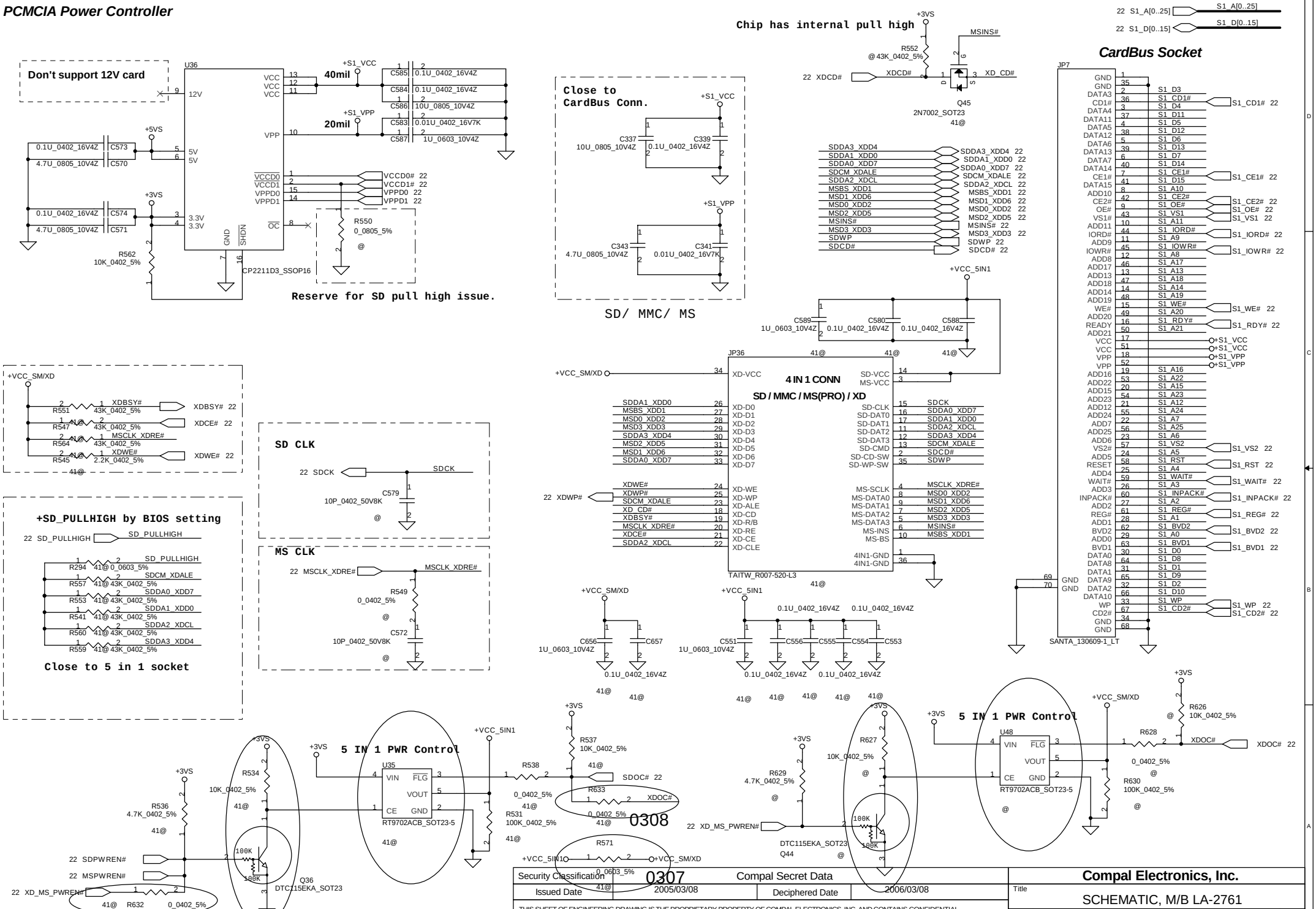
PCMCIA Power Controller



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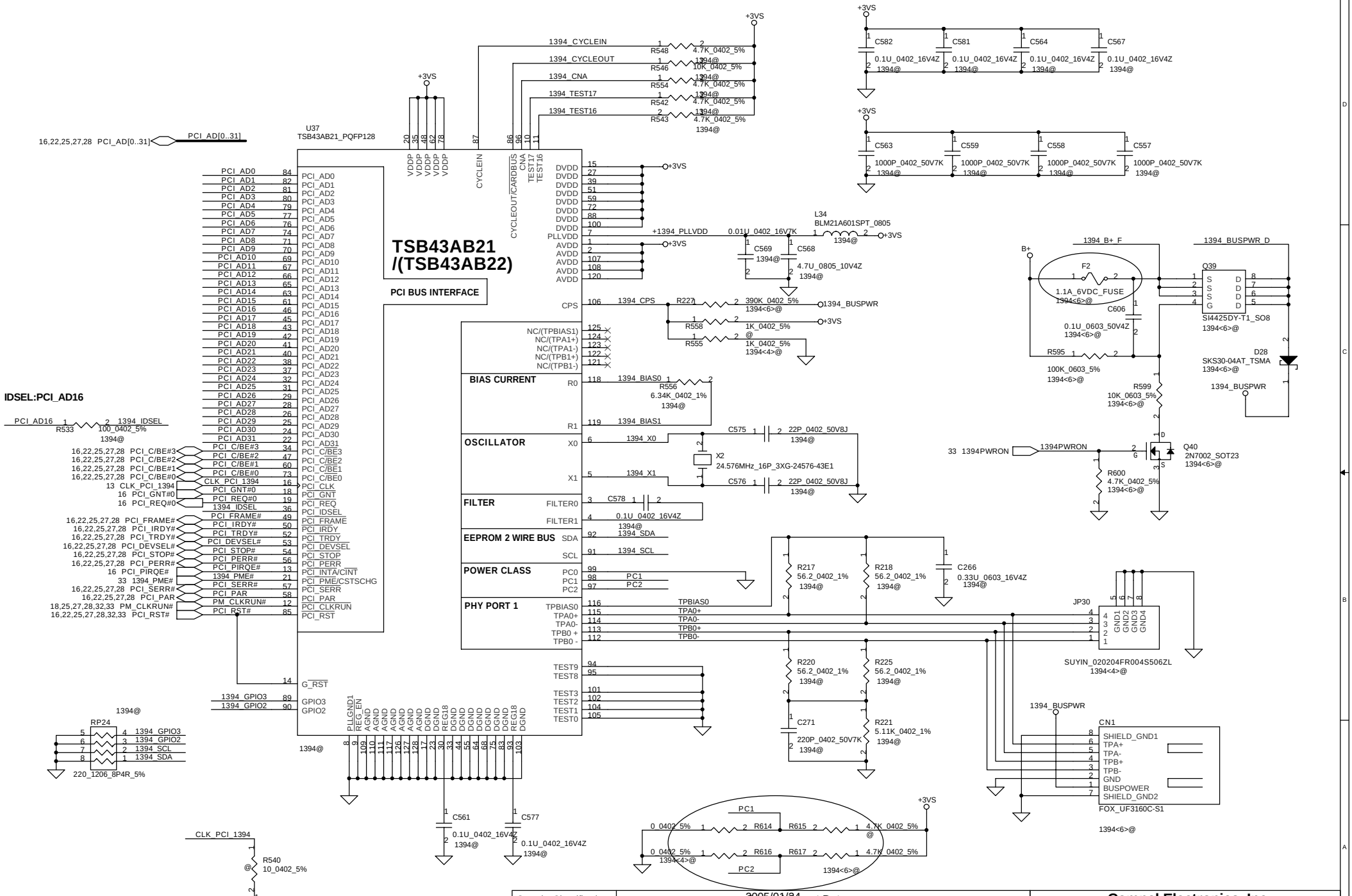
TSB43AB21
/(TSB43AB22)
PCI BUS INTERFACE
U37
TSB43AB21_PQFP128
IDSEL:PCI_AD16
BIAS CURRENT
OSCILLATOR
FILTER
EEPROM 2 WIRE BUS
POWER CLASS
PHY PORT 1
1394_CYCLEIN
1394_CYCLEOUT
1394_CNA
1394_TEST17
1394_TEST16
PCI_AD[0..31]
+3VS
+1394_PLLVDD
1394_BUSPWR
1394_B+_F
1394_BUSPWR_D
1394PWRON
SI4425DY-T1_SO8
SKS30-04AT_TSMA
2N7002_SOT23
SUYIN_020204FR004S506ZL
FOX_UF3160C-S1
CN1
JP30
RP24
220_1206_8P4R_5%
X2
24.576MHz_16P_3XG-24576-43E1
L34
BLM21A601SPT_0805
1.1A_6VDC_FUSE
PC1
PC2
CLK_PCI_1394
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2005/01/24
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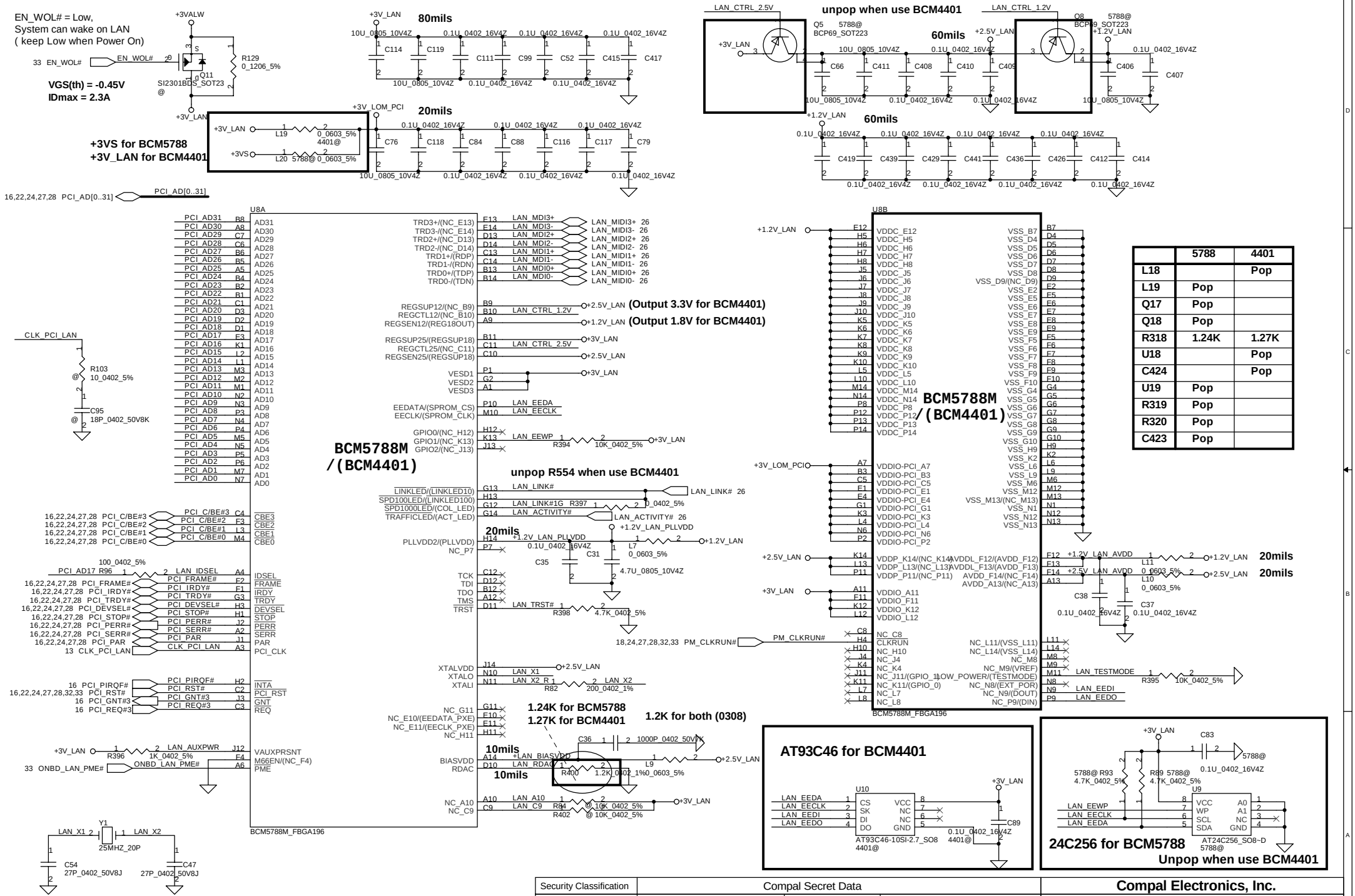

	5788	4401
L18		Pop
L19	Pop	
Q17	Pop	
Q18	Pop	
R318	1.24K	1.27K
U18		Pop
C424		Pop
U19	Pop	
R319	Pop	
R320	Pop	
C423	Pop	

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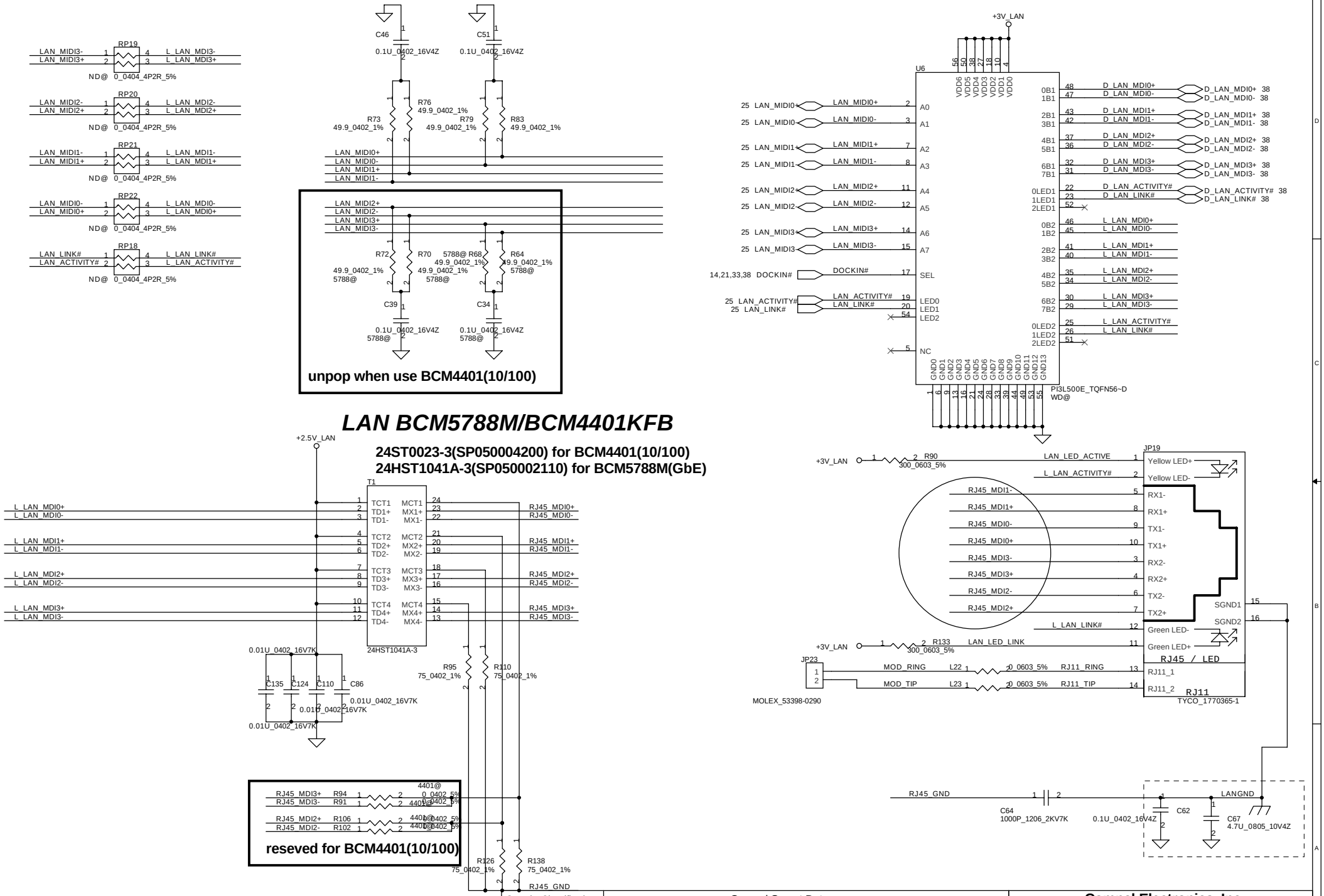

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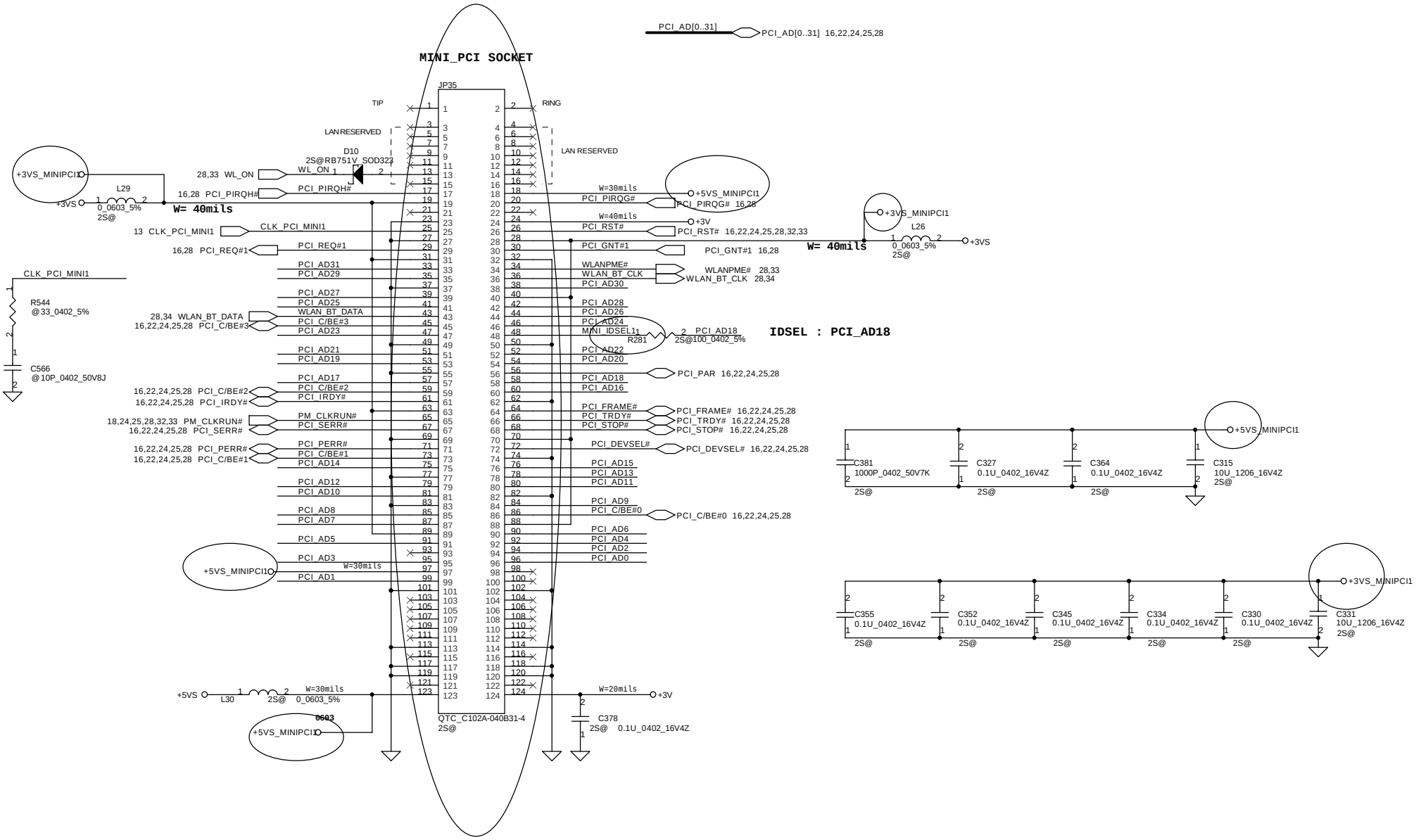

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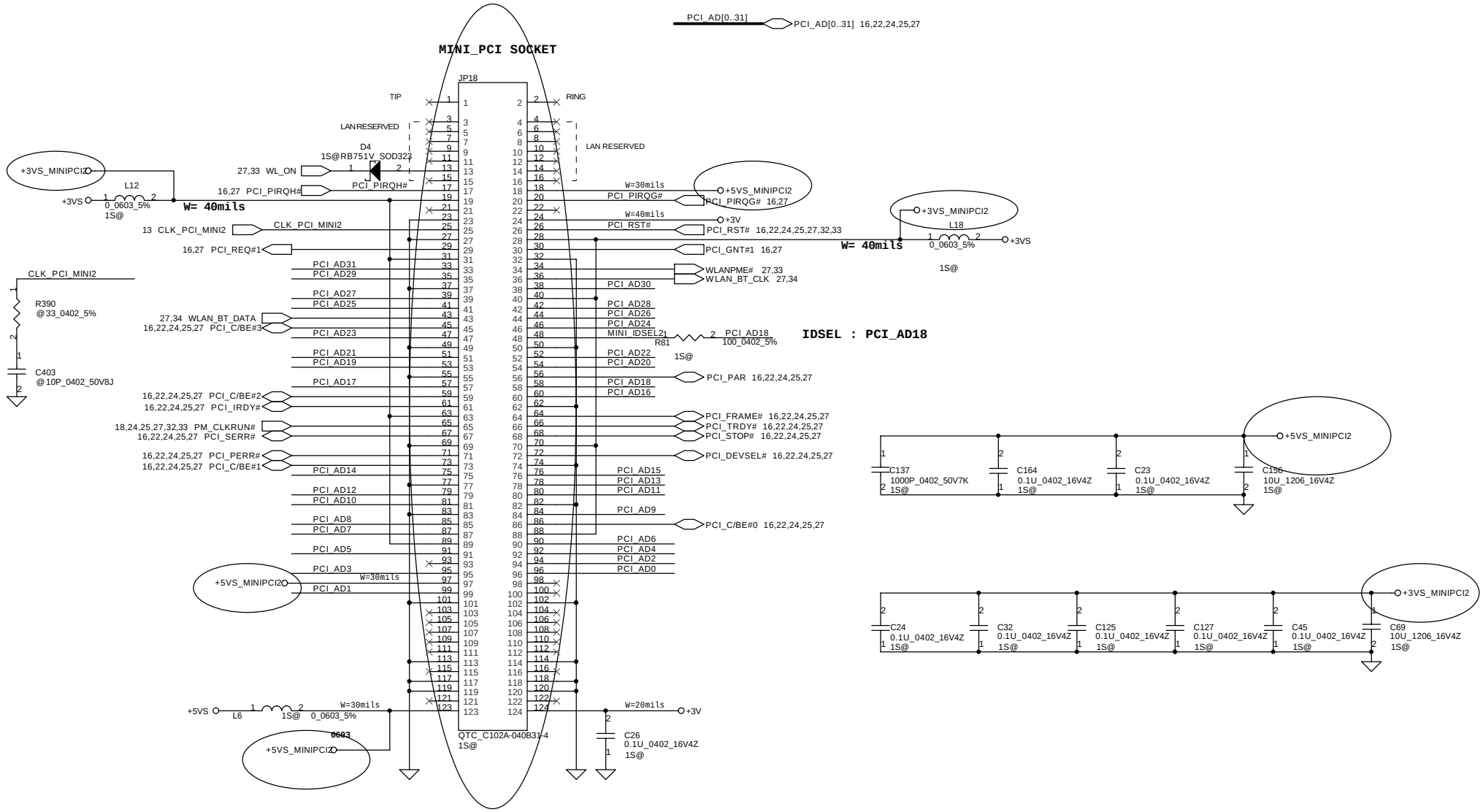

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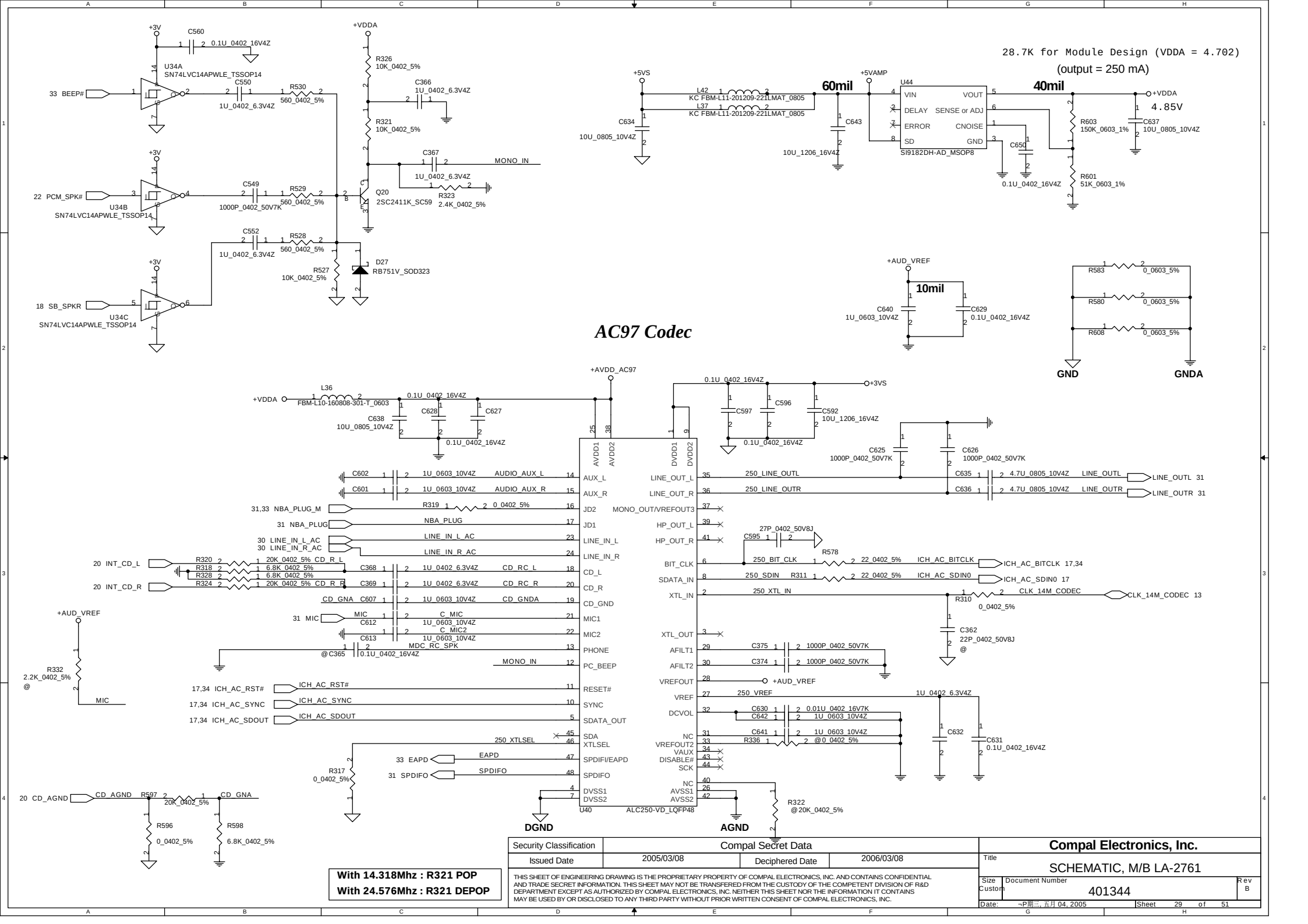

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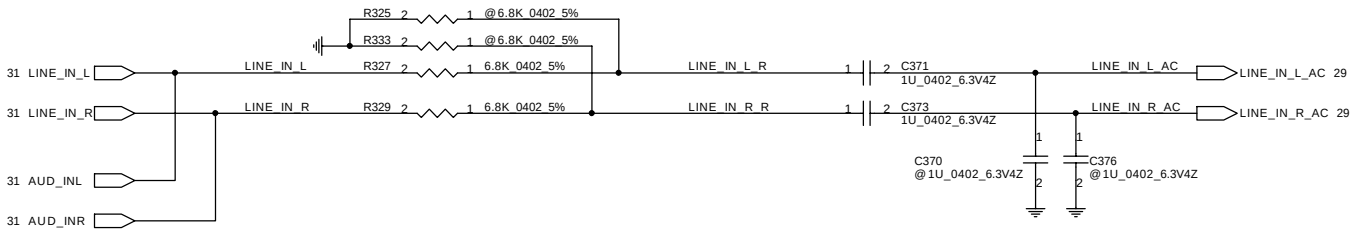

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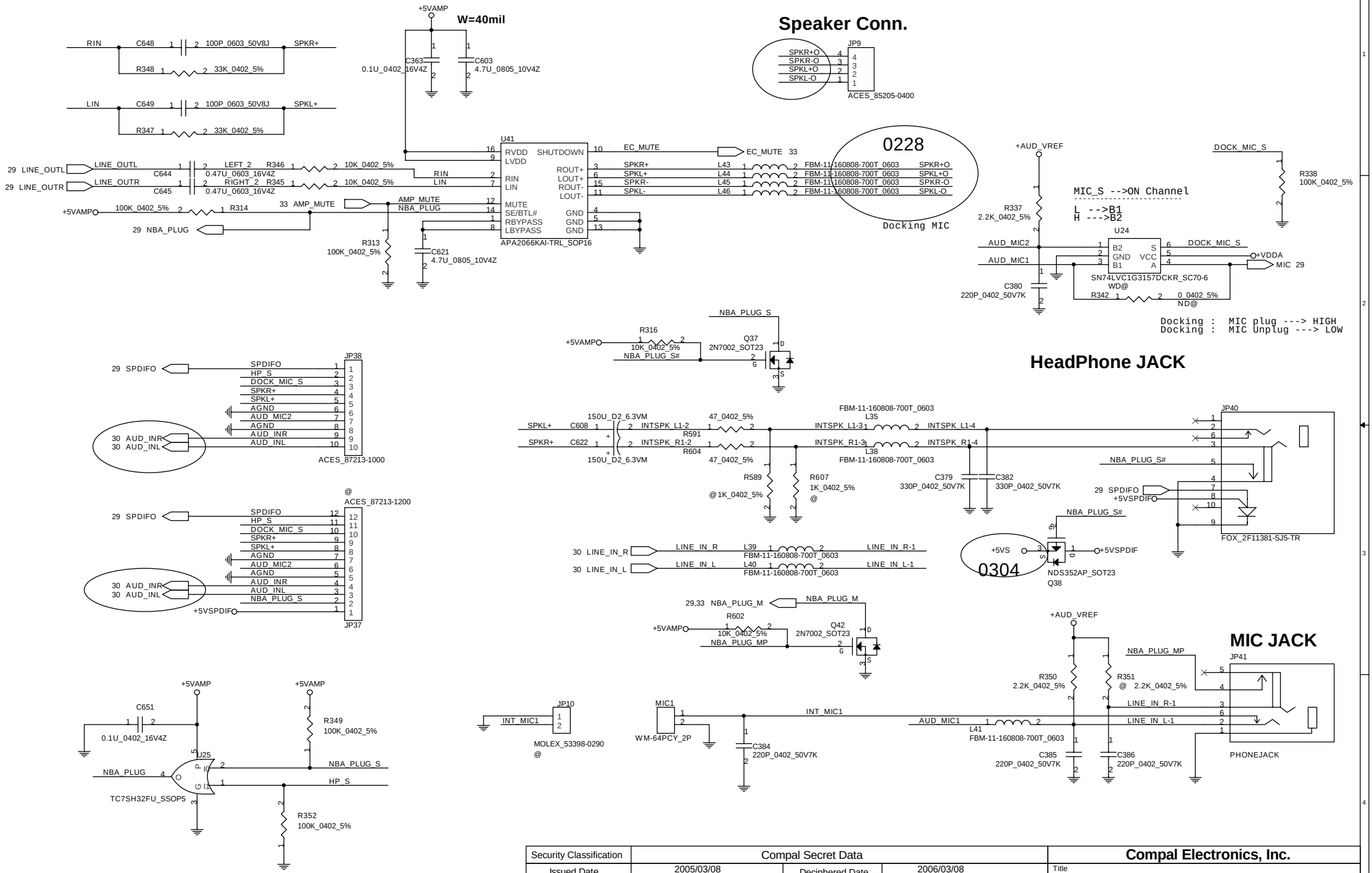

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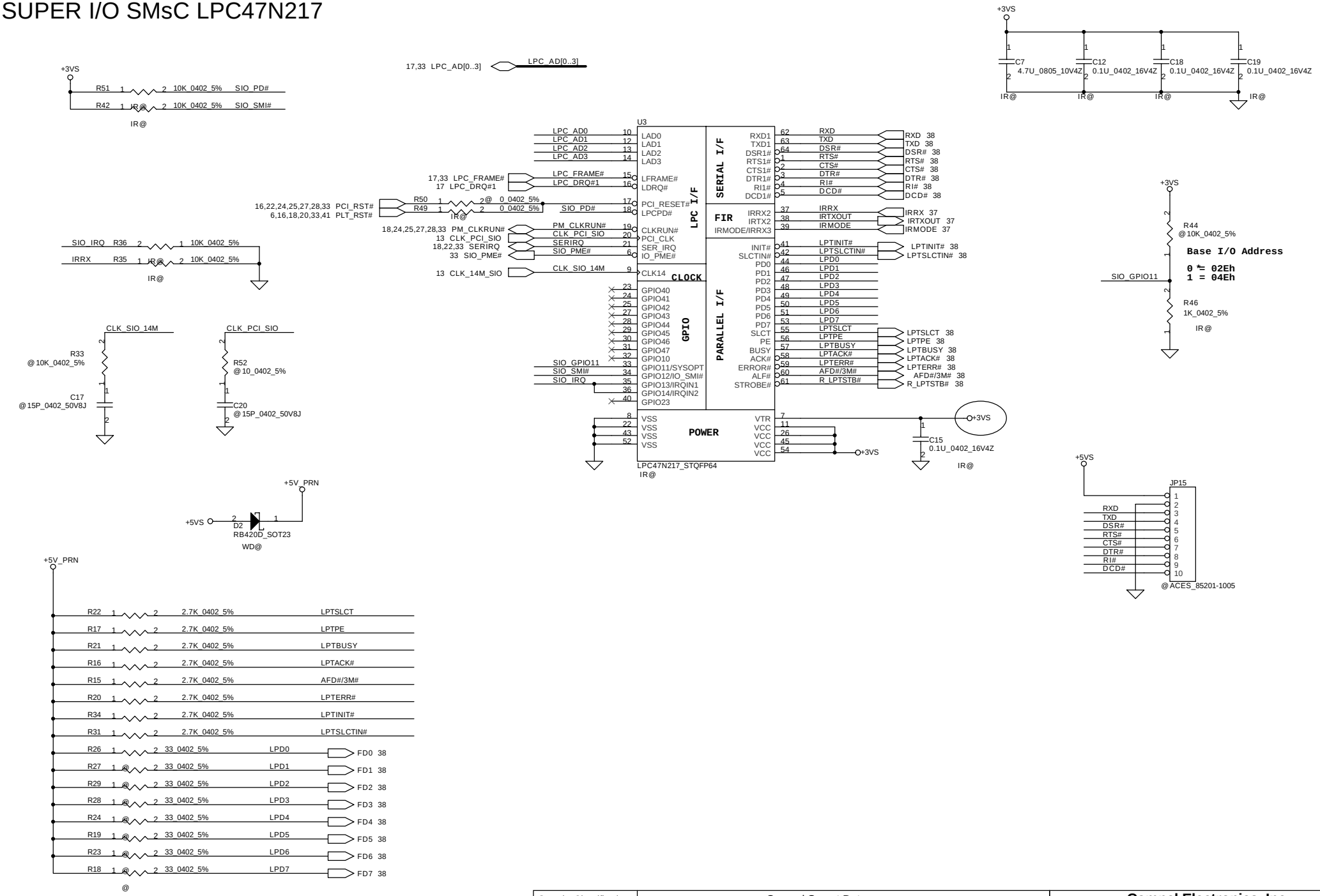
SUPER I/O SMsC LPC47N217



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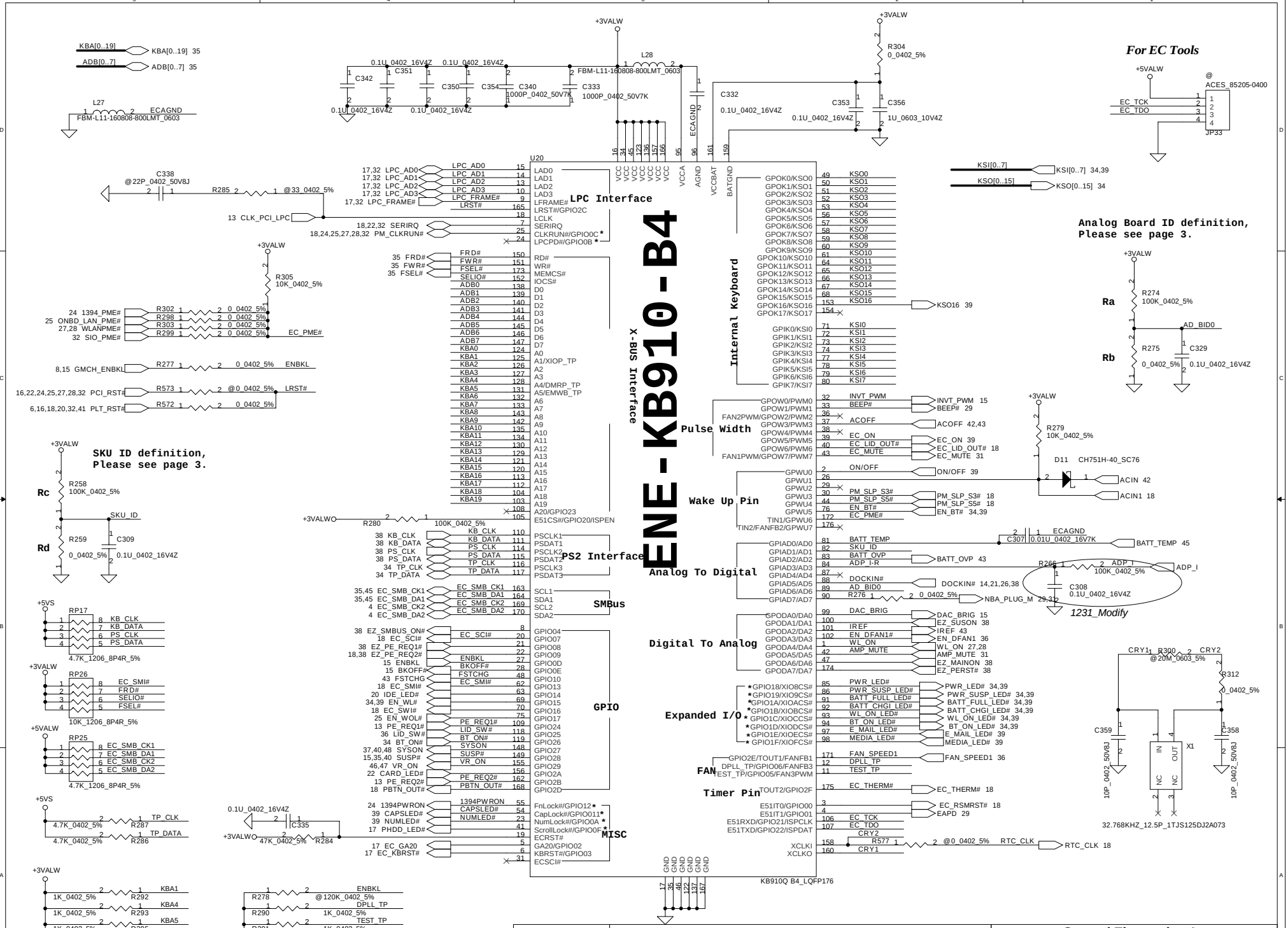

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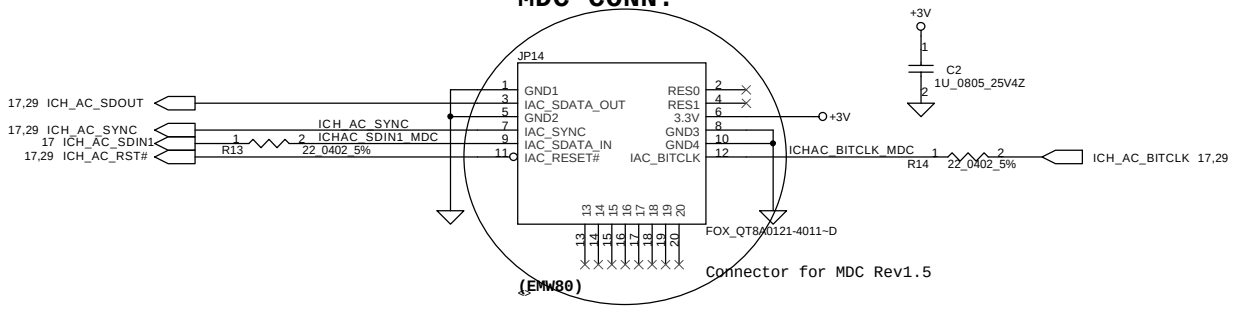
MDC CONN.



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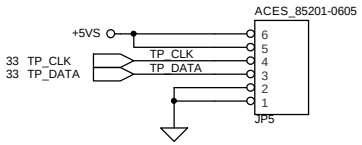

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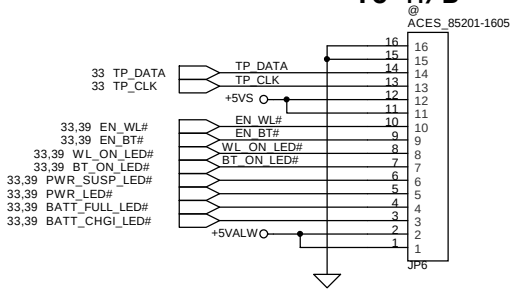

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KSO[0..15] — KSO[0..15] 33

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KSI3	C217	100P_0402_25V8K
KSO9	C220	100P_0402_25V8K
KSI2	C222	100P_0402_25V8K
KSI1	C224	100P_0402_25V8K
KSO10	C227	100P_0402_25V8K
KSO11	C233	100P_0402_25V8K
KSI0	C235	100P_0402_25V8K
KSO12	C237	100P_0402_25V8K
KSO13	C239	100P_0402_25V8K
KSO14	C241	100P_0402_25V8K
KSO15	C242	100P_0402_25V8K

KSI7	C238	100P_0402_25V8K
KSI6	C236	100P_0402_25V8K
KSI5	C234	100P_0402_25V8K
KSO0	C232	100P_0402_25V8K
KSO1	C226	100P_0402_25V8K
KSO2	C223	100P_0402_25V8K
KSI4	C221	100P_0402_25V8K
KSO3	C218	100P_0402_25V8K
KSO4	C216	100P_0402_25V8K
KSO5	C214	100P_0402_25V8K
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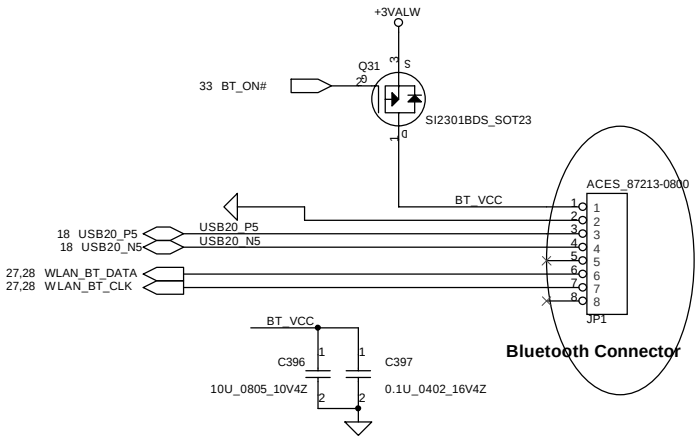
KSO7	C212	100P_0402_25V8K

BlueTooth Interface



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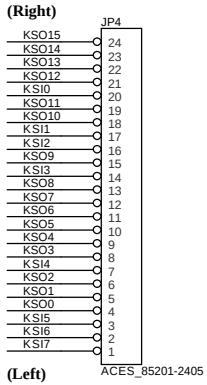

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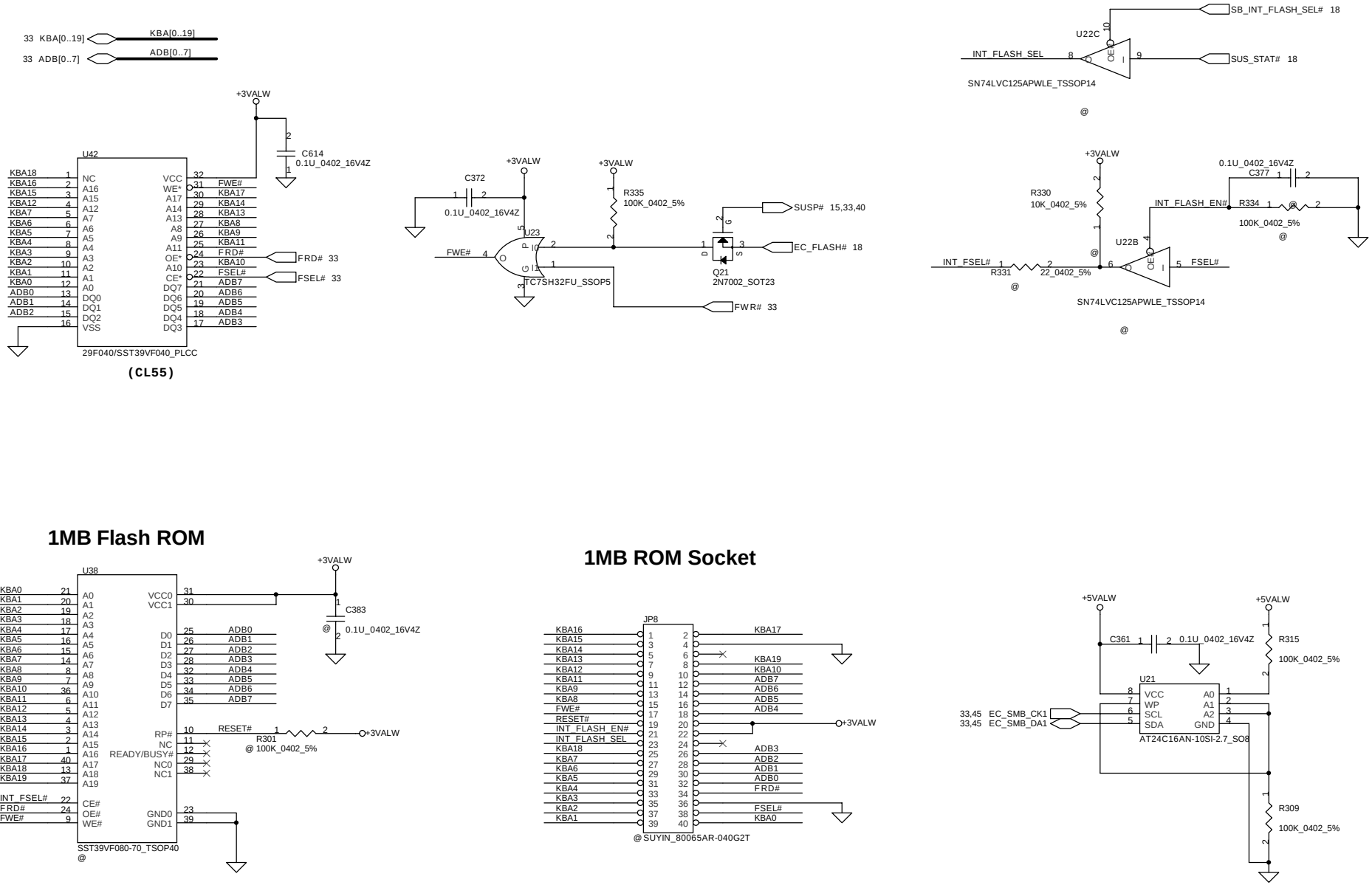

1MB Flash ROM

1MB ROM Socket

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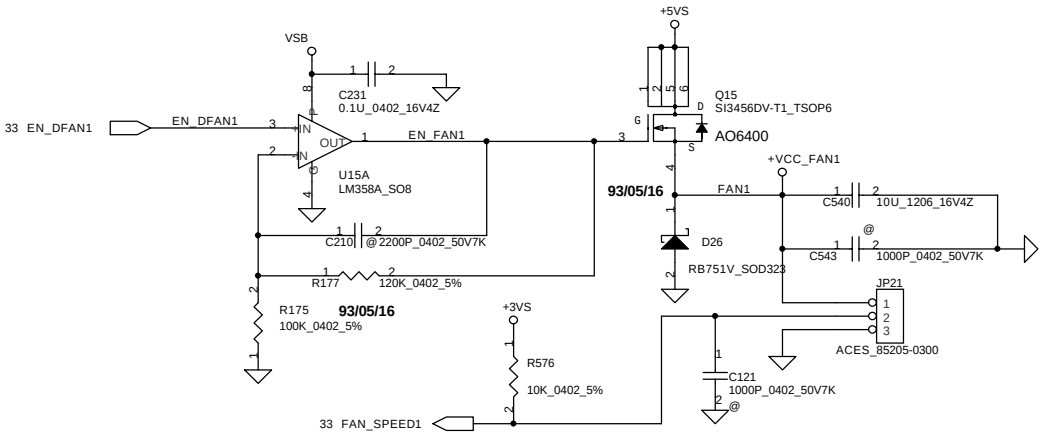
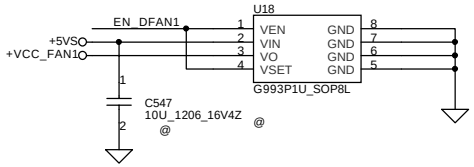
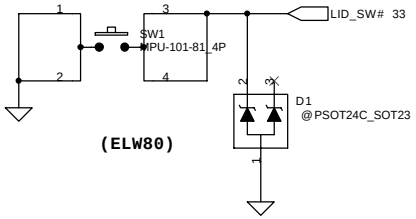
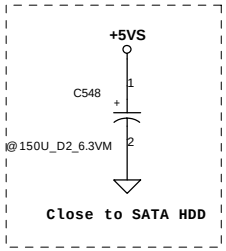
FAN Conn









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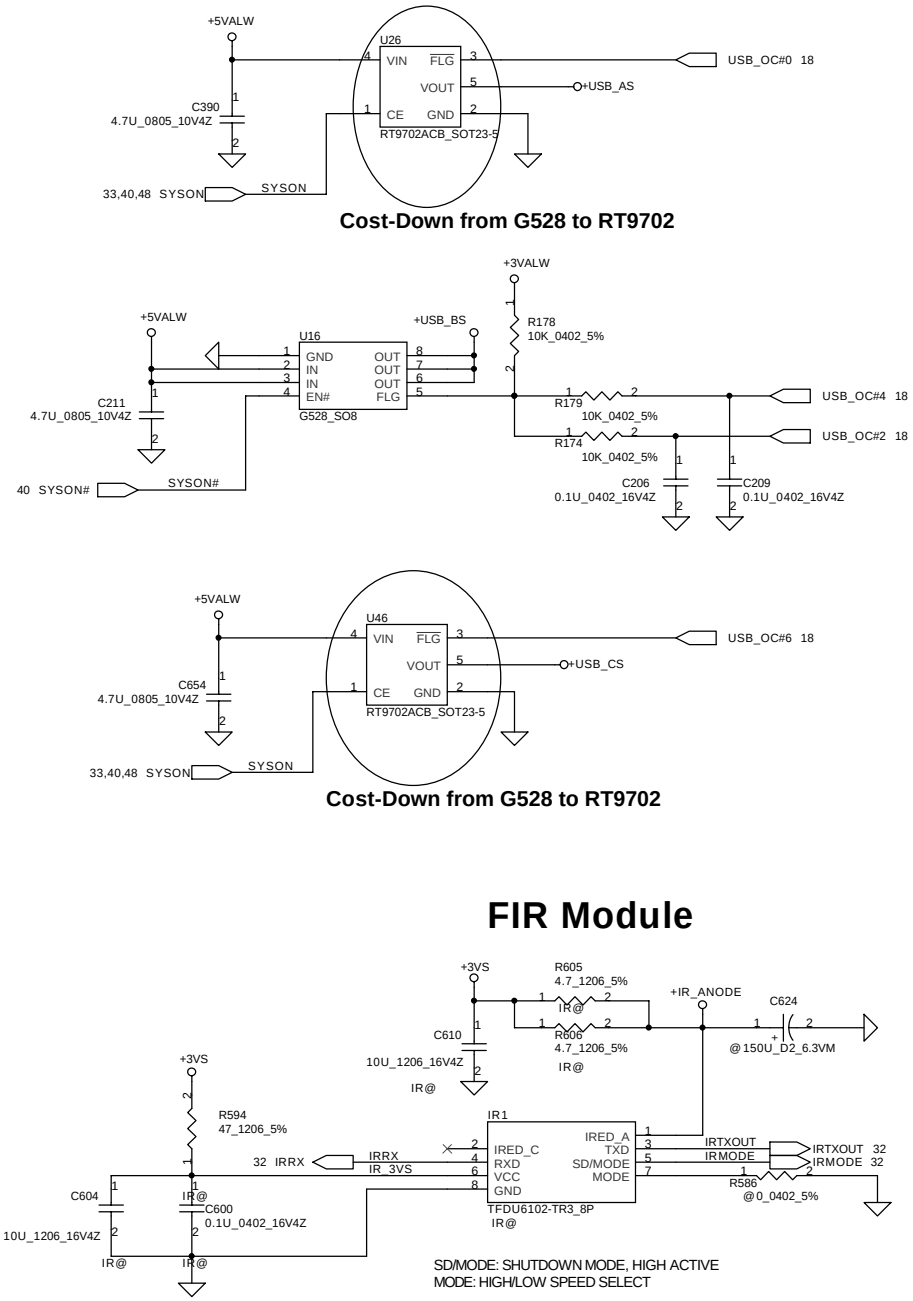

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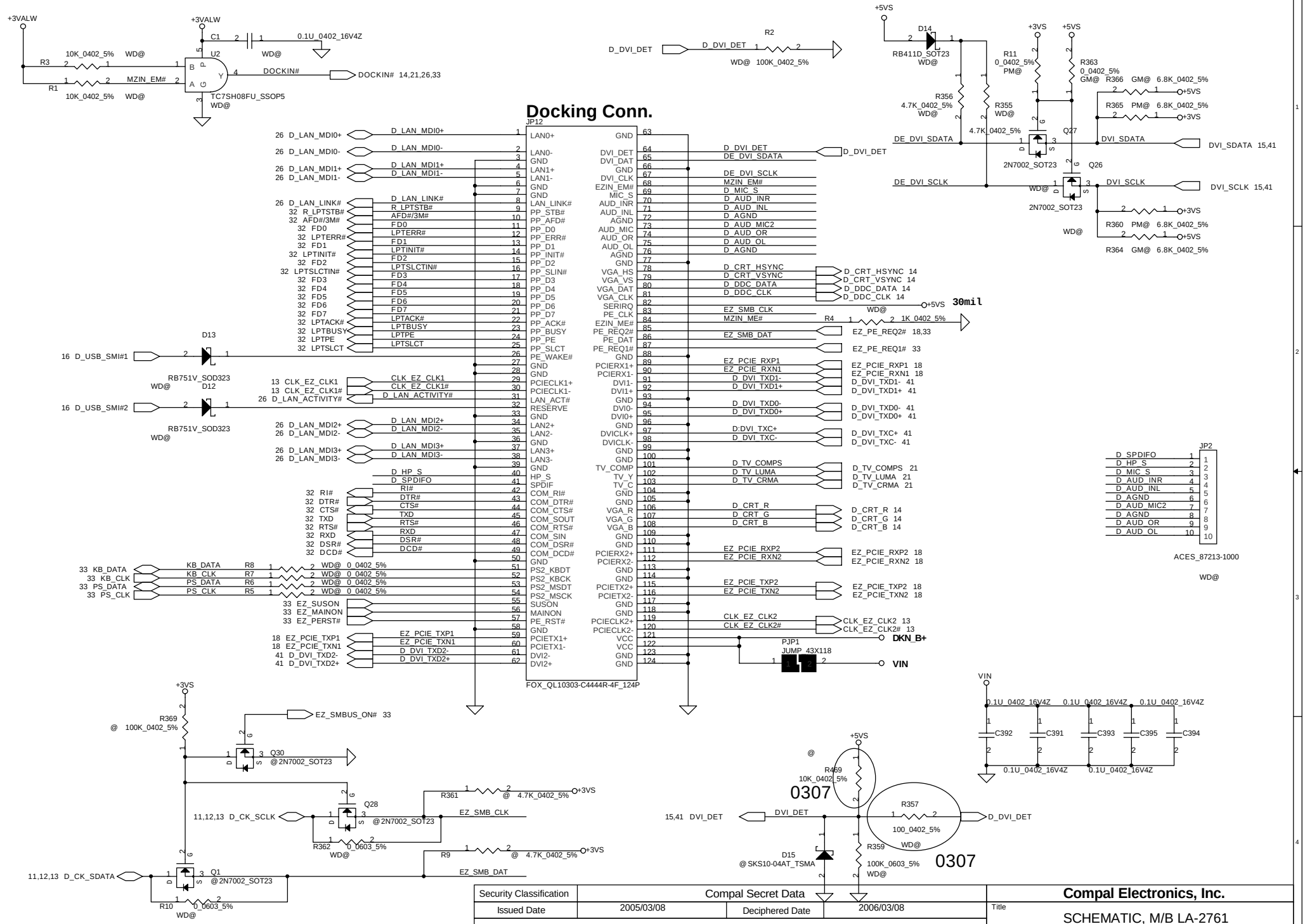

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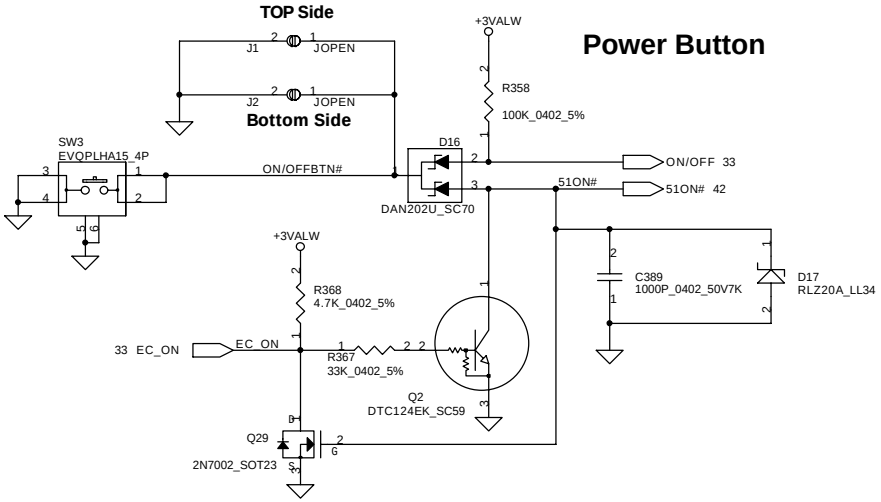

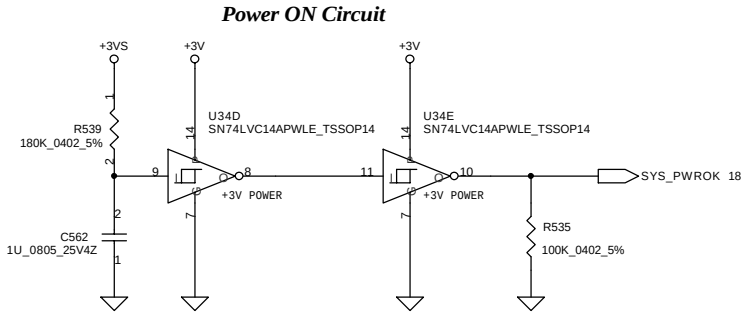

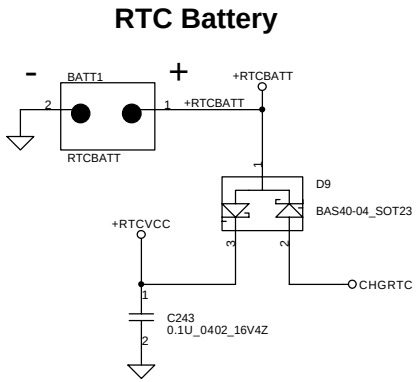

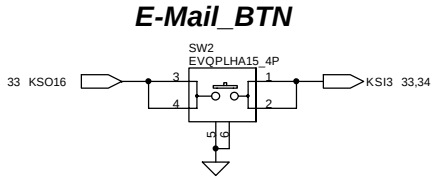

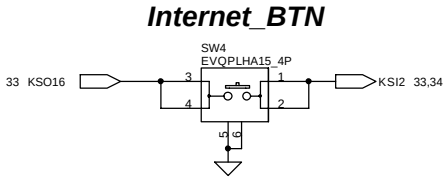

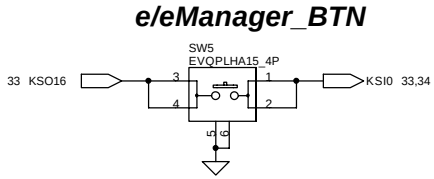

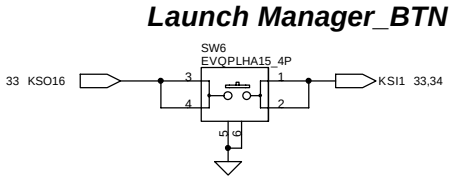

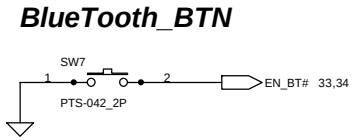

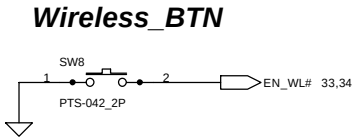

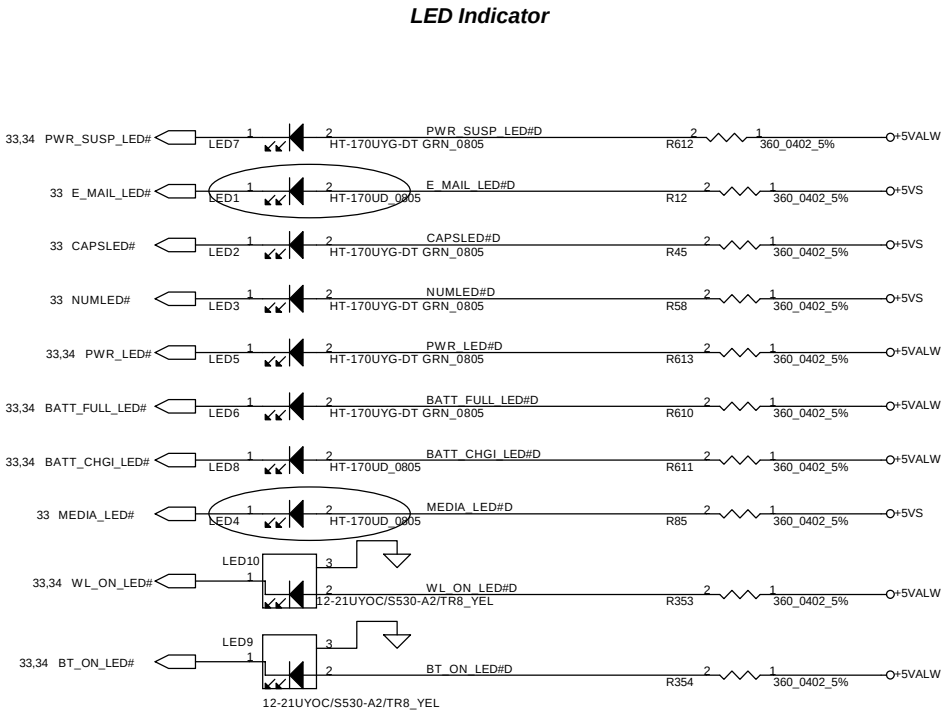

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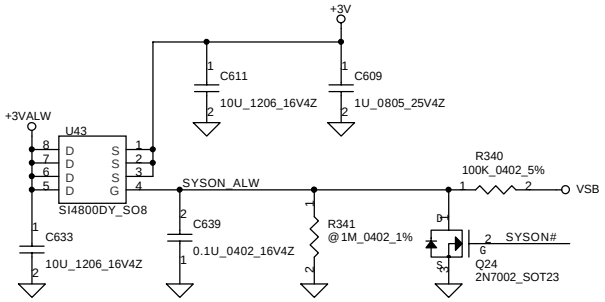
+3VALW TO +3V



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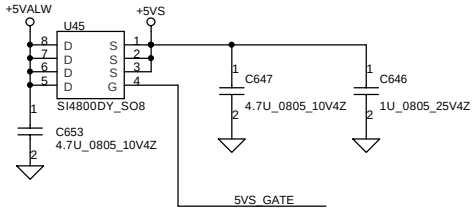

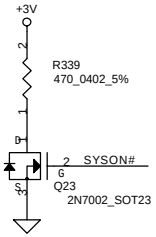

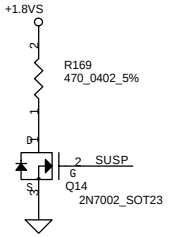

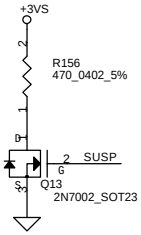

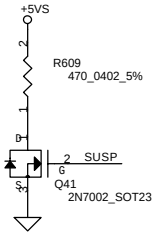

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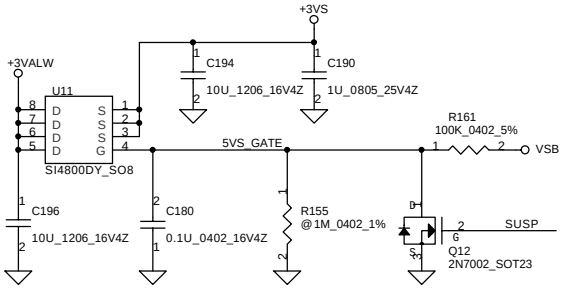

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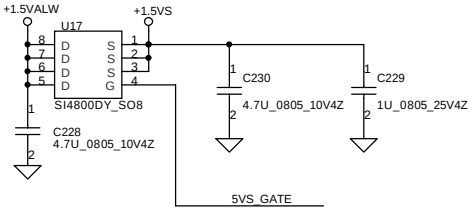

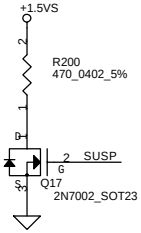

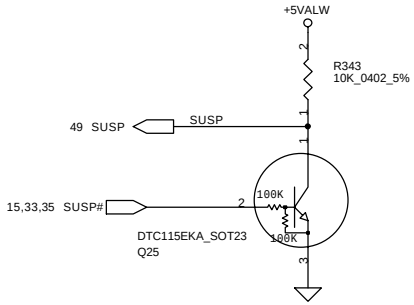

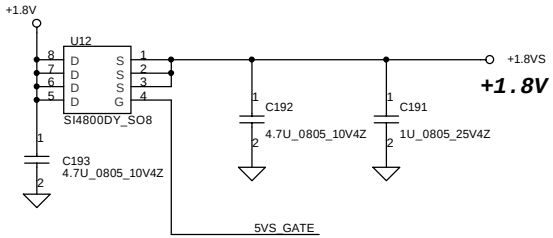

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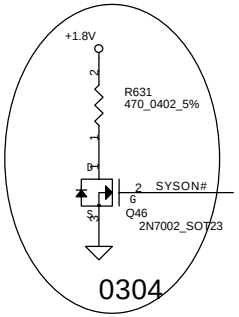

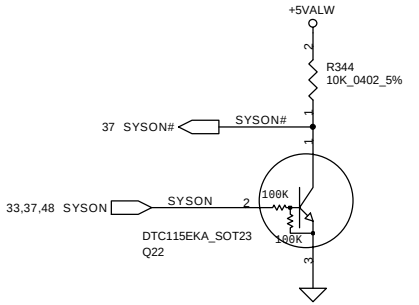

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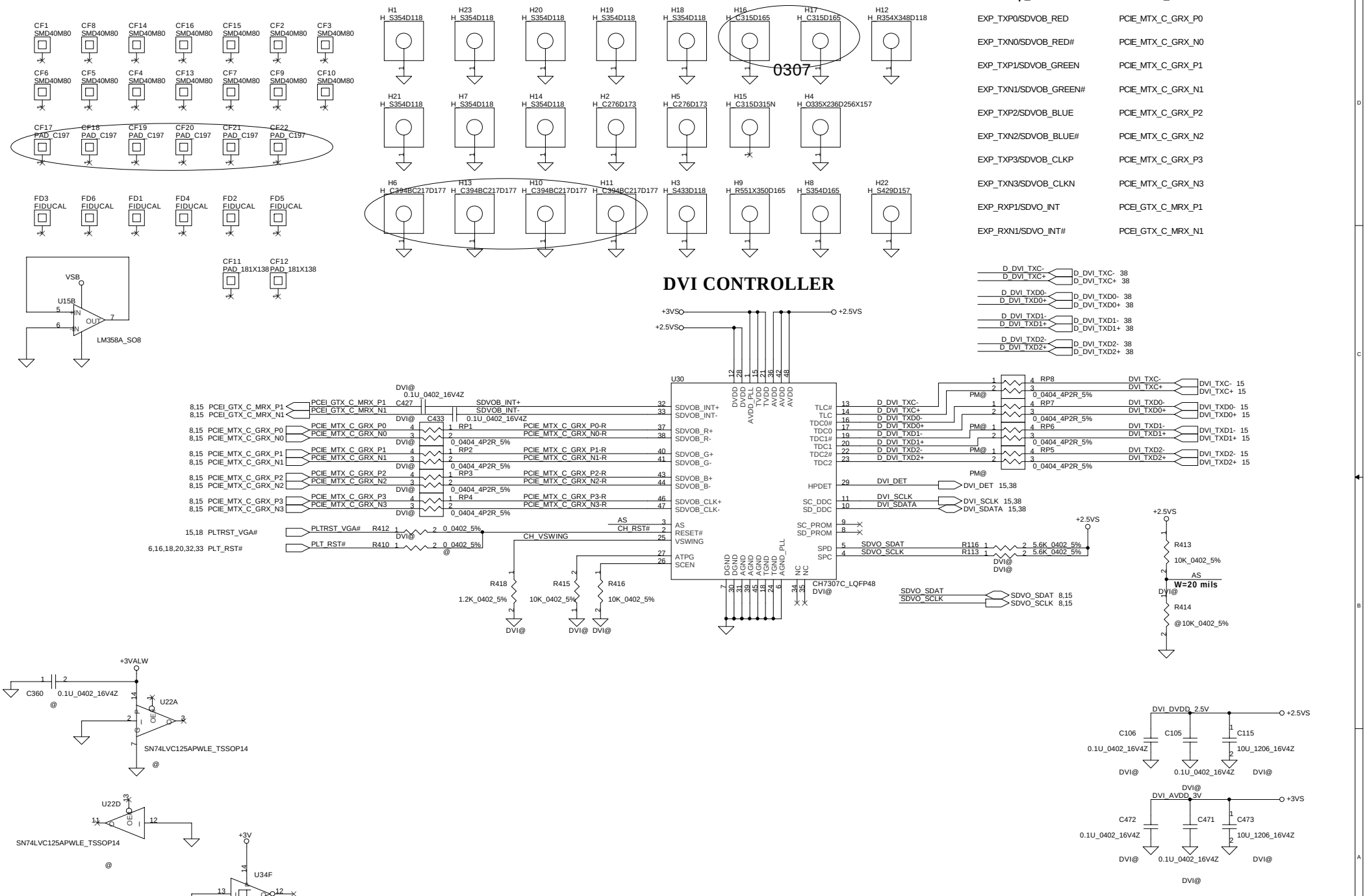

Chip_Name	Label_Name
EXP_TXP0/SDVOB_RED	PCIE_MTX_C_GRX_P0
EXP_TXN0/SDVOB_RED#	PCIE_MTX_C_GRX_N0
EXP_TXP1/SDVOB_GREEN	PCIE_MTX_C_GRX_P1
EXP_TXN1/SDVOB_GREEN#	PCIE_MTX_C_GRX_N1
EXP_TXP2/SDVOB_BLUE	PCIE_MTX_C_GRX_P2
EXP_TXN2/SDVOB_BLUE#	PCIE_MTX_C_GRX_N2
EXP_TXP3/SDVOB_CLKP	PCIE_MTX_C_GRX_P3
EXP_TXN3/SDVOB_CLKN	PCIE_MTX_C_GRX_N3
EXP_RXP1/SDVO_INT	PCEI_GTX_C_MRX_P1
EXP_RXN1/SDVO_INT#	PCEI_GTX_C_MRX_N1

Security Classification	Compal Secret Data	
Issued Date	2005/03/08	Deciphered Date 2006/03/08

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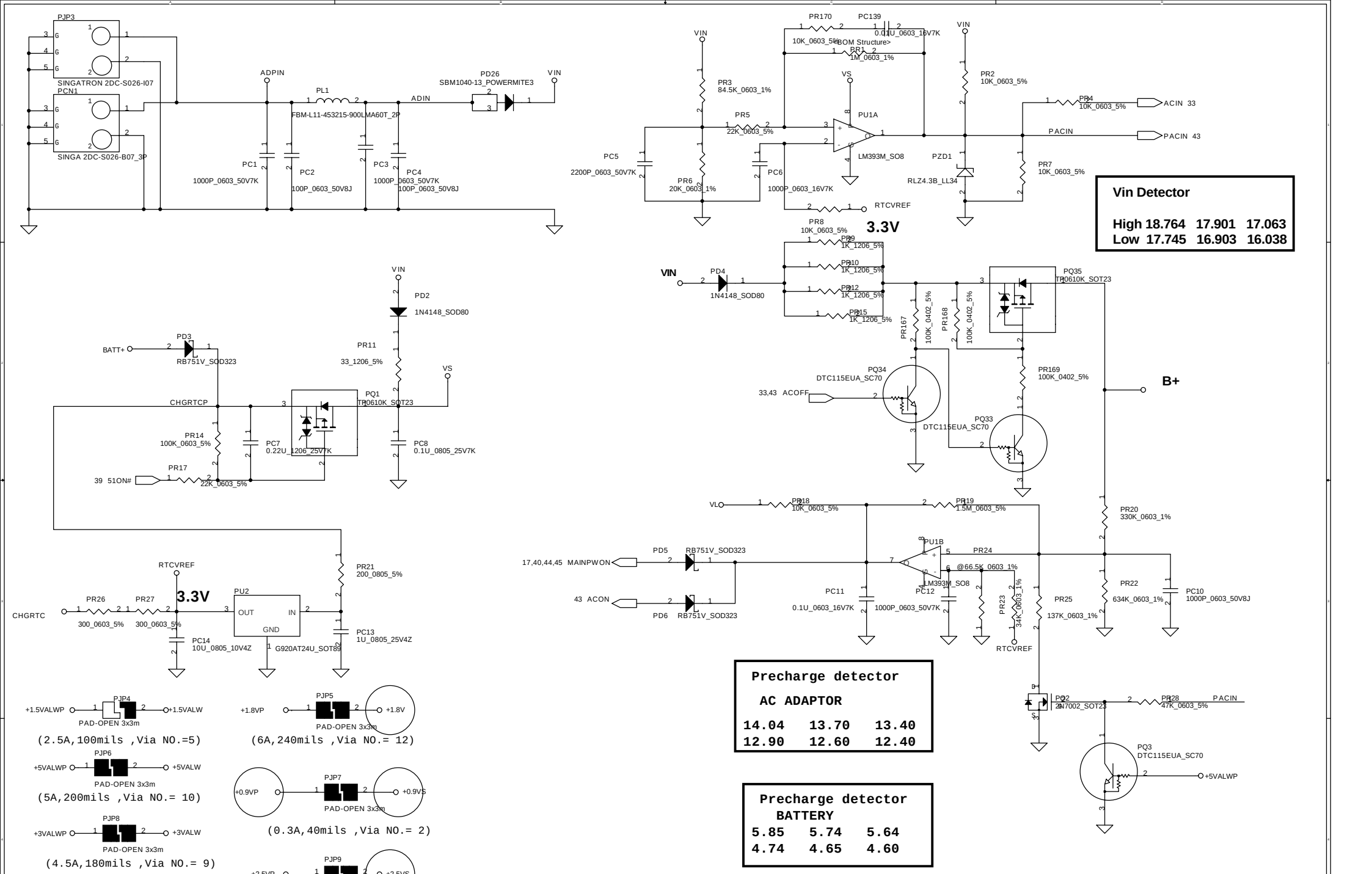

Vin Detector

High	18.764	17.901	17.063
Low	17.745	16.903	16.038

Precharge detector
AC ADAPTOR

14.04	13.70	13.40
12.90	12.60	12.40

Precharge detector
BATTERY

5.85	5.74	5.64
4.74	4.65	4.60

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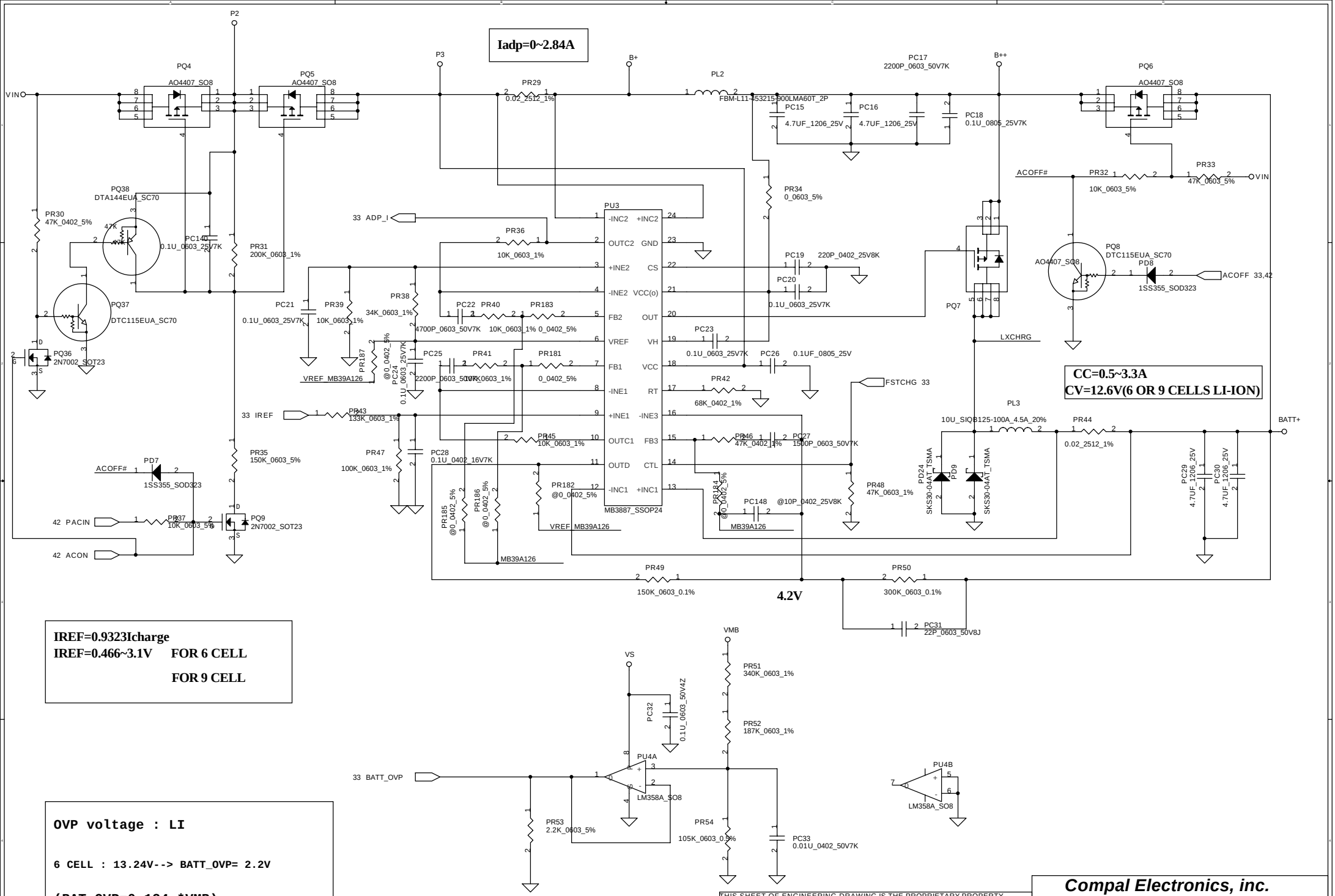

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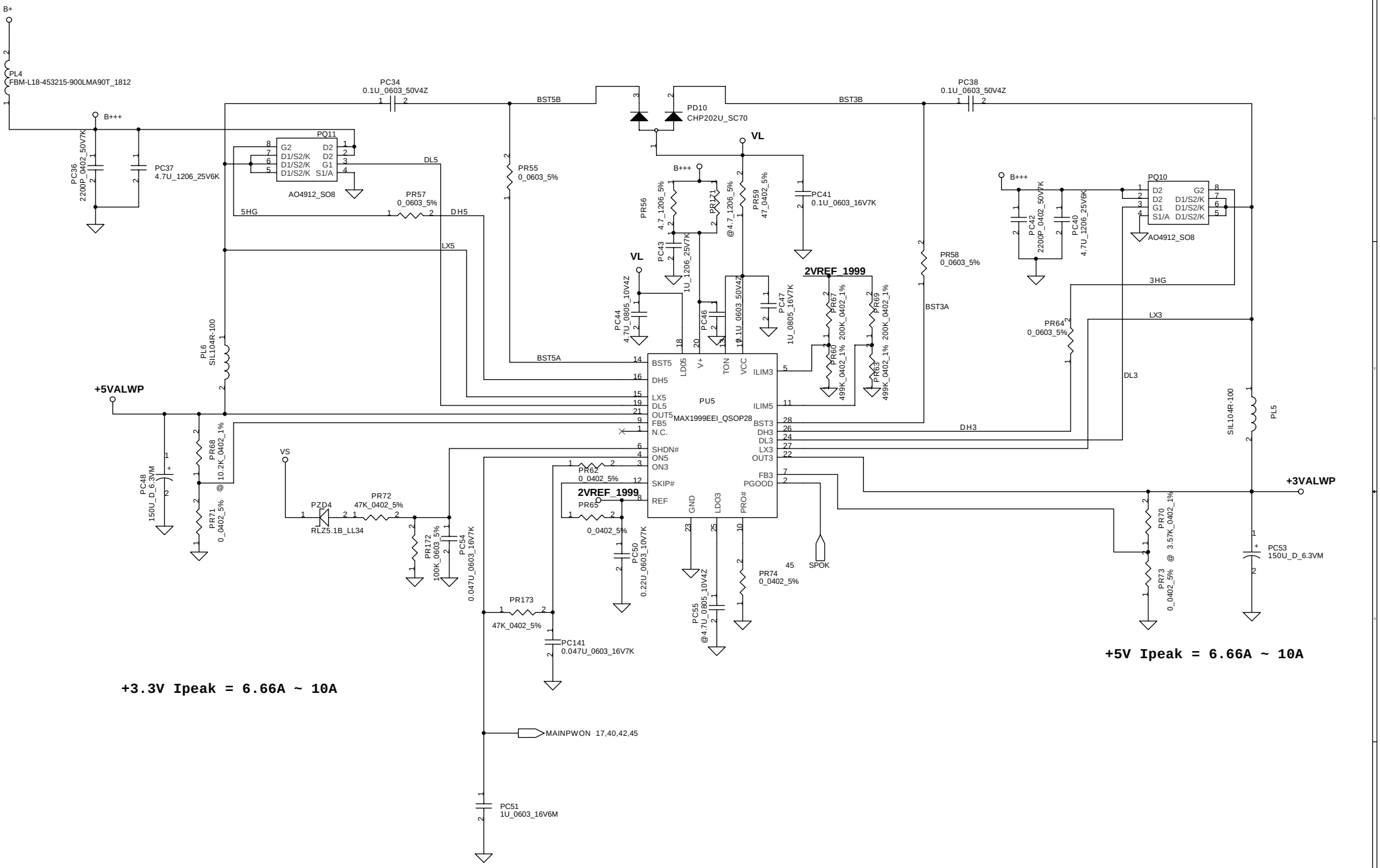

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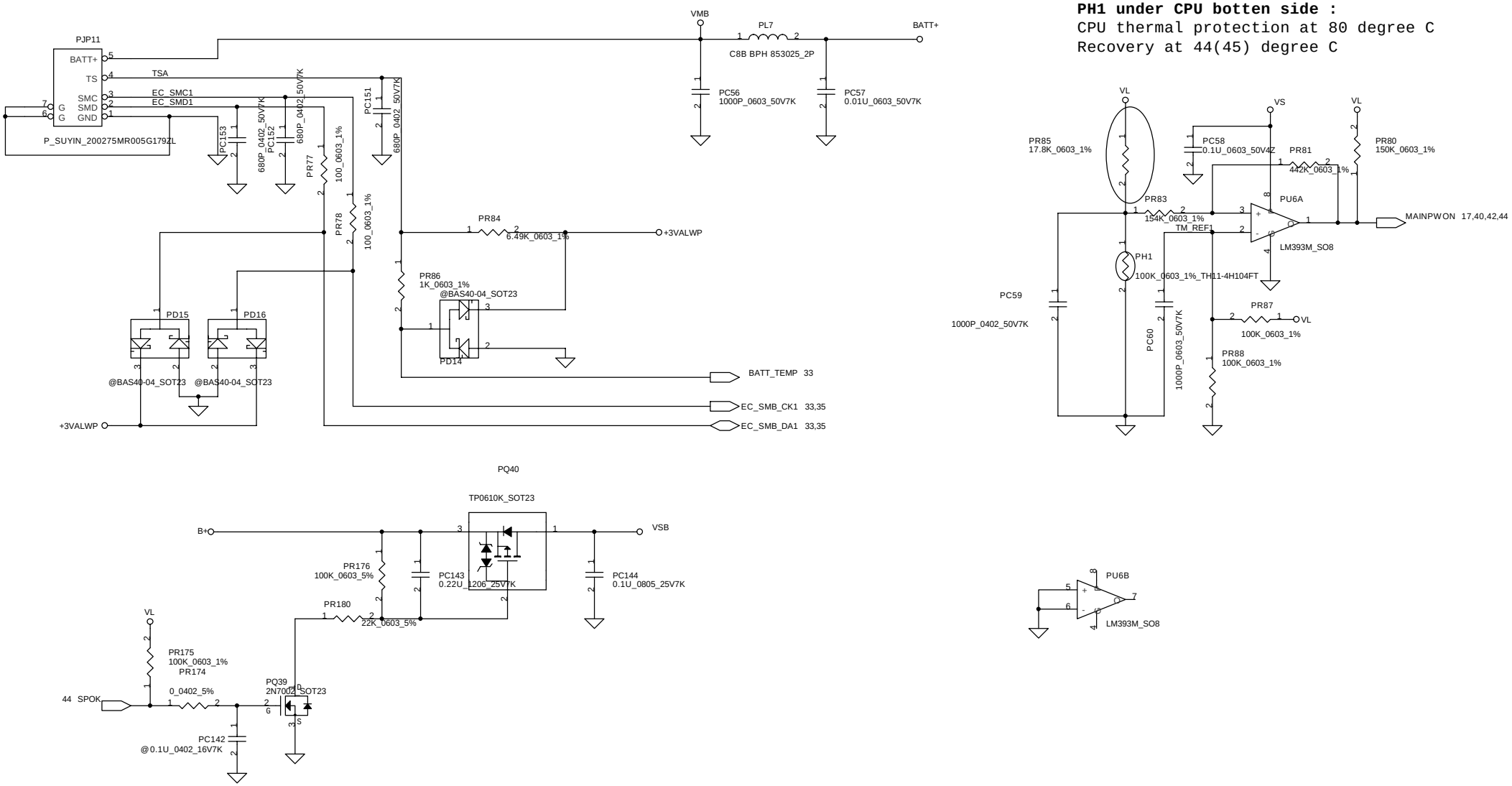
PH1 under CPU botten side :
CPU thermal protection at 80 degree C
Recovery at 44(45) degree C



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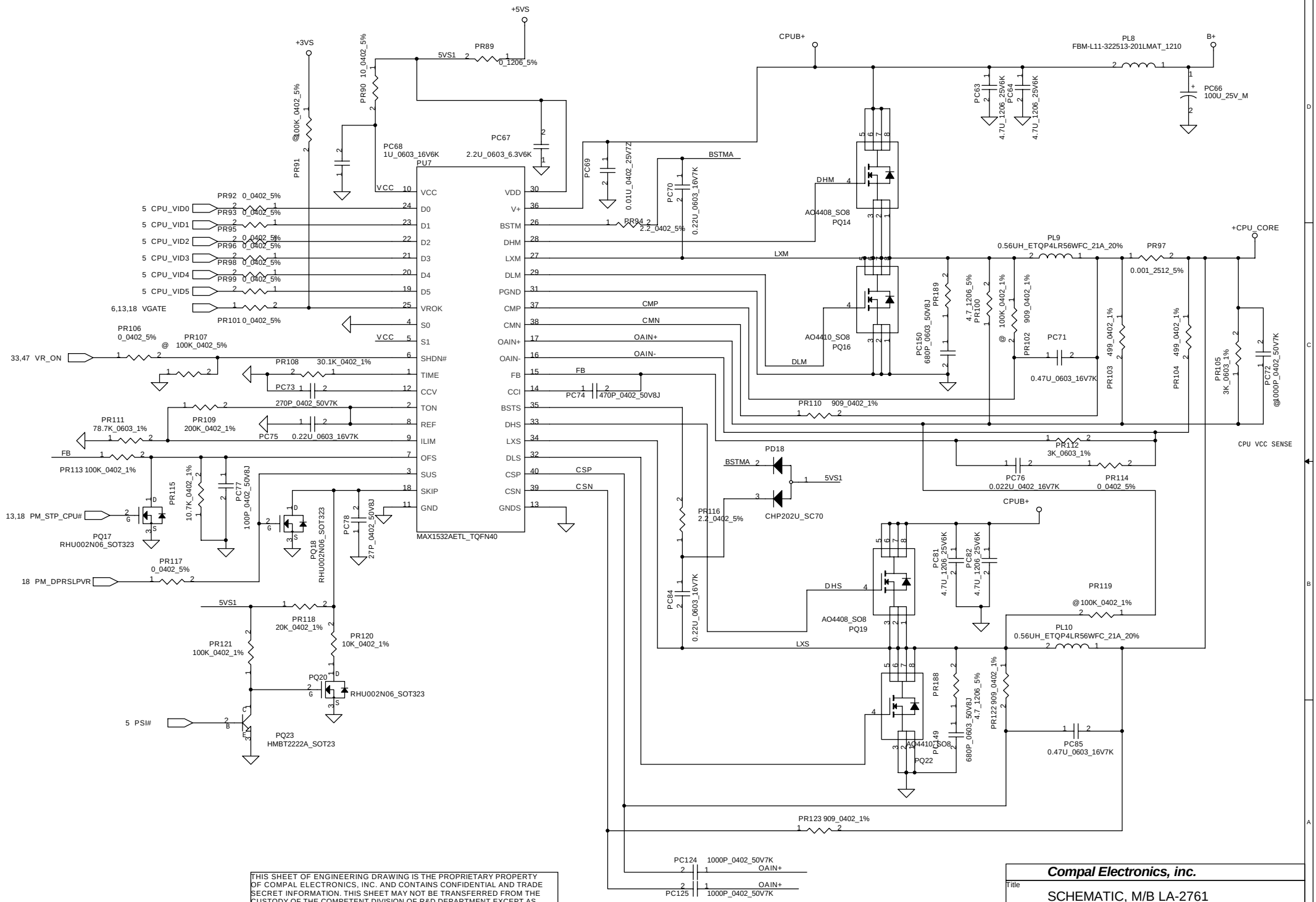

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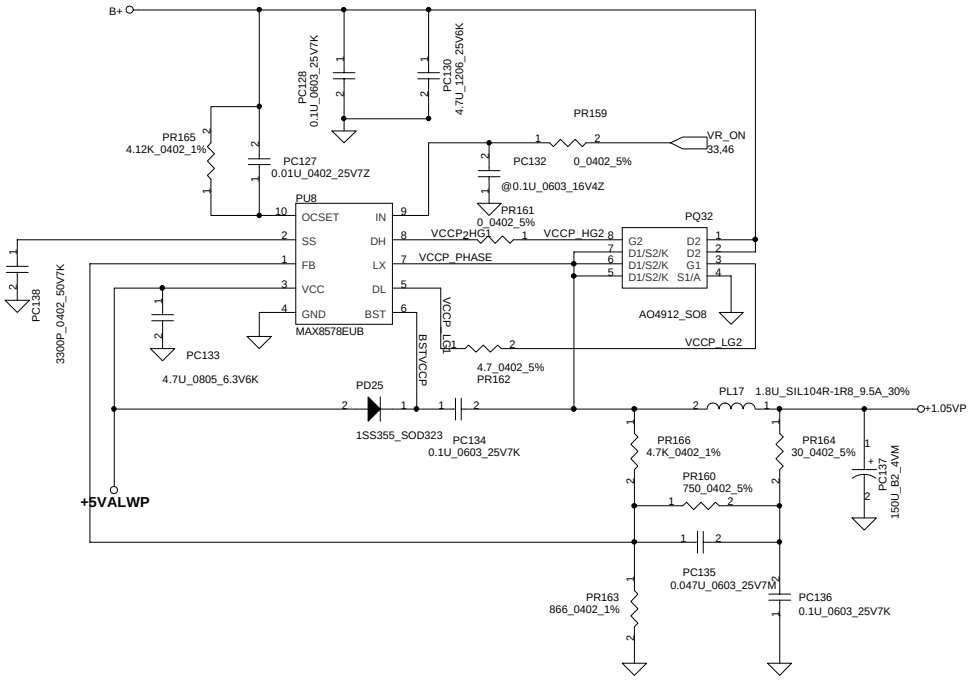

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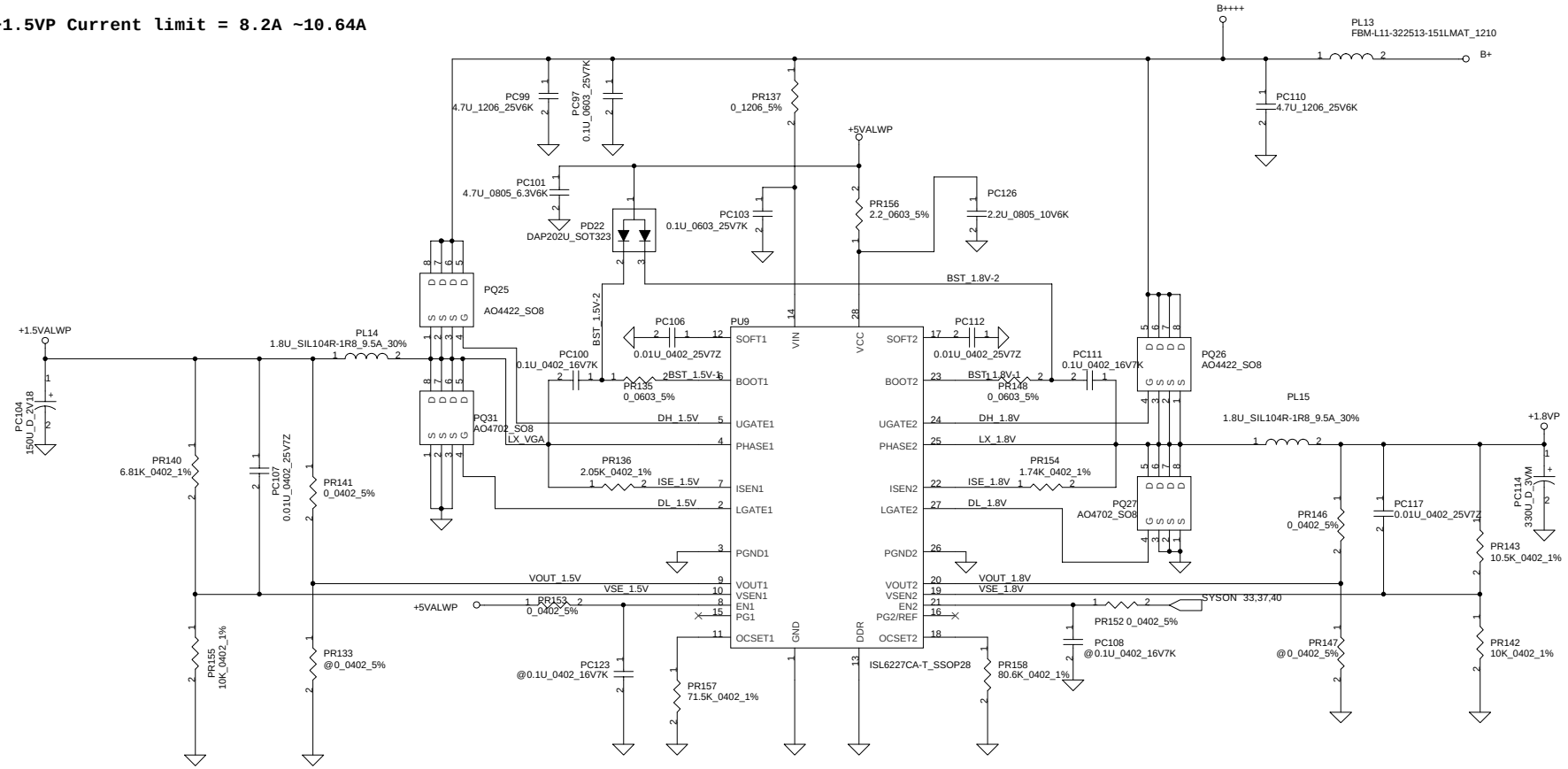
+1.8VP O.C.P. =8.1A ~ 10.36A

+1.5VP Current limit = 8.2A ~10.64A



915PM(DISCRETE)	**PR143=11K 1.8VP=1.867V**
915GM (UMA)	**PR143=10.5K 1.8VP=1.8V**

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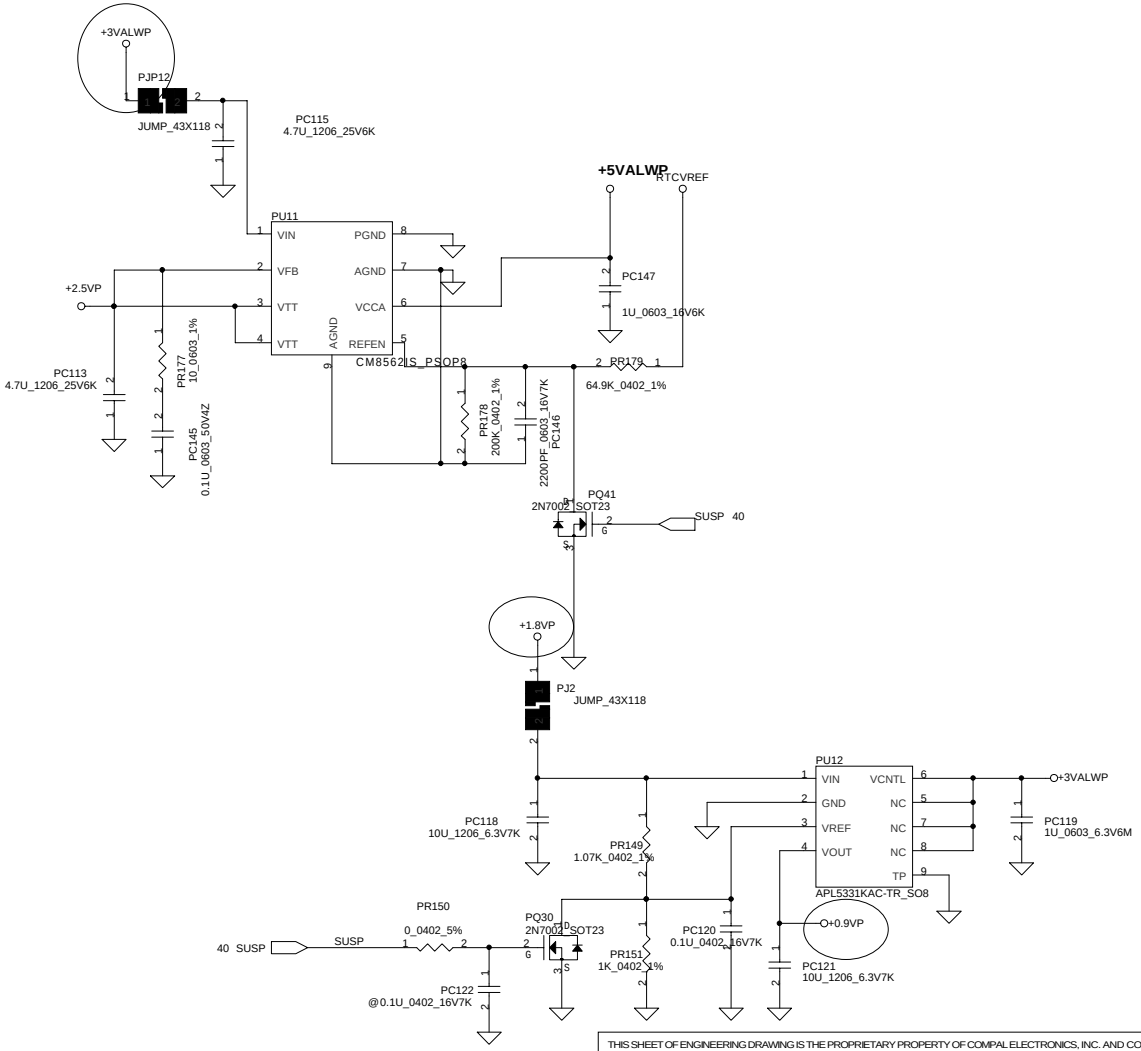

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1	Delete R45,R47	EMI cost down	0.2	28			
2	Add R505,C627	Improve signal quality					
3							
4							
5							
6							
7							
8							
9							

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1		Modify PU8 IC		47	1. change PU8 from MAX8576 to MAX8578 2delete PC132		DVT
2		Modify 1.05VP voltage level		47	1. change PR166 from 7.15k to 4.7k , PC135 from 6800P to 0.047u 0603		DVT
3		change precharge detect point		42	1. change PR20 from 412k to 330k		DVT
		Modify disable precharge respond time		42	1. change PR167/PR168/PR169 from 470k to 100k		DVT
		PD16 PIN2 AND PIN3 are wrong		45	1. modify PD16 schematic,and delete PD16(only reserve)		DVT
		for decrease BATT connector EMI		45	1. add PC151/PC152/PC153 :680PF		DVT
		for decrease CPU CORE switching ring effect and add EMI solution : snubber		46	1. change PR94/PR116 from 0 to 2.2 2. add PR189//PR188 4.7 1206 ,add PC150/PC149 680P		DVT
4							
5							
6							
7							
8							
9							

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